AI/ML ROLE IN RTL DESIGN GENERATION

28 January 2025

Meeting hosted by Open Research Institute, Inc., San Diego Chapter of IEEE Information Theory Society, and the San Diego Section IEEE Local Group ***Open Source Digital Radio****.*

WHERE DO WE START?

- Identify and discuss core concepts
- Discuss a few selected works
- Recommend literature, tools, standards, and frameworks

CORE CONCEPTS

- Electronic Design Automation
  - Computer based tools, workflows, and processes used to specify, implement and verify electronic design - ASICs, FPGAs, PCBs, modules, systems and sub-systems - examples
    - RTL designs, simulation and synthesis
    - ASIC/FPGA placement and routing
      - Closing timing - meeting performance objectives
- Design Risk
  - Three types of risk in electronic design
    - Schedule risk - missing design milestones
      - Estimate 2 weeks for an RTL module, and it actually took 5 weeks
    - Technical risk - missing design capabilities
      - Targeting a clock rate of 500 MHz, but only able to achieve 400 MHz.
    - Cost risk - missing design cost requirements
      - Area estimate is too low, requires a larger die or larger FPGA

CORE CONCEPTS

- Design Process
  - Iterative - Design, simulate, synthesis, place and route - does it meet timing?
    - Finding design deficiencies and identifying incorrect assumptions early in the design process saves time and effort.
      - Changing RTL to fix timing errors found in place and route is inefficient and a significant source of schedule risk

CORE CONCEPTS

FPGA Design Process	AI/ML Opportunities
System Specification	Determination of design requirements, standards research
System Architecture and Partitioning	HLS, design space exploration, timing closure prediction
RTL Design And Verification	RTL generation, verification
FPGA Implementation (Synthesis, PnR)	Synthesis, placement, routing, timing closure
System Validation	Test generation, test automation

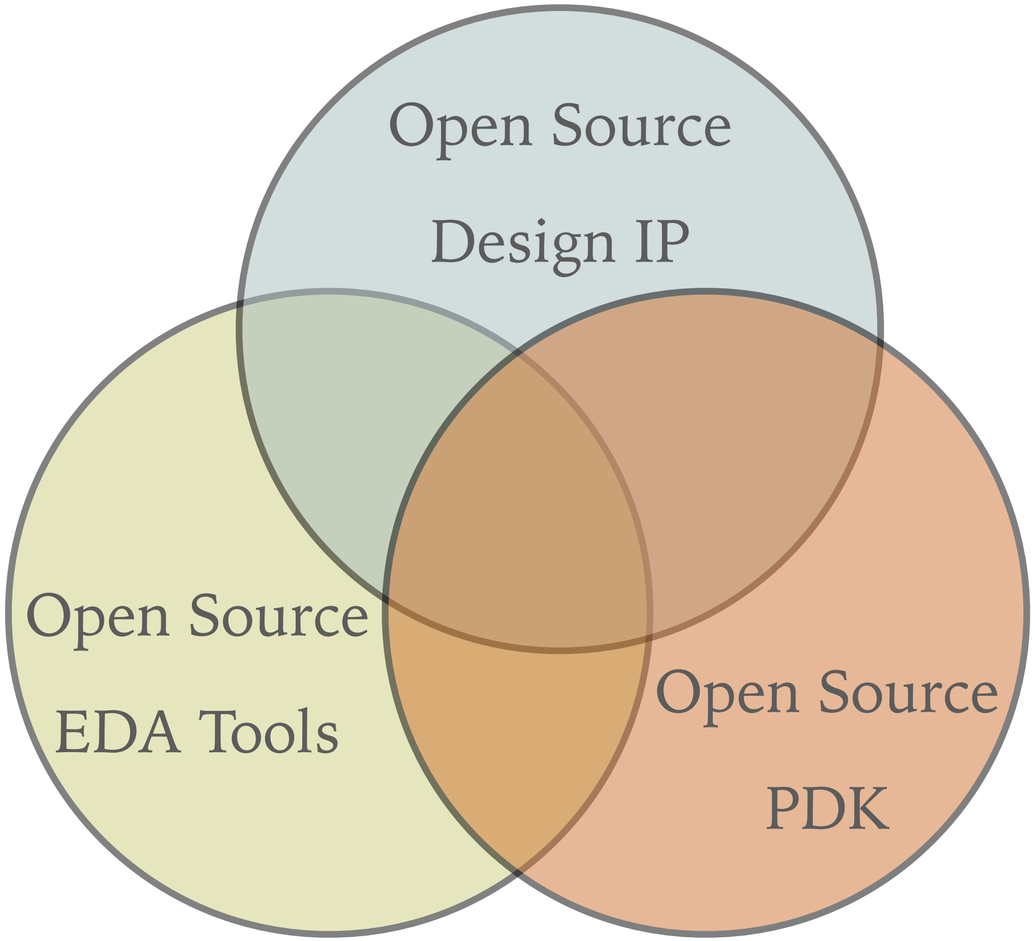
SELECTED WORKS

- "Recommendations and Roadmap for Open-Source EDA in Europe" from the FOSSi Foundation. This document can be found here: https://fossi-foundation.org/resources/eu-roadmap
- Access to EDA software is traditionally limited and costly
- There is a workforce shortage
- Collaboration, innovation, and lowered barriers to entry - can they be achieved with Open Source along with AI/ML?
- Starting in 2015, open source design IP got a big boost from RISC-V
- An Open Source Process Design Kit (PDF) for Google Skywater in 2020 (130nm)
- Accessible manufacturing capacity and EDA tools (Open Road, UCSD)

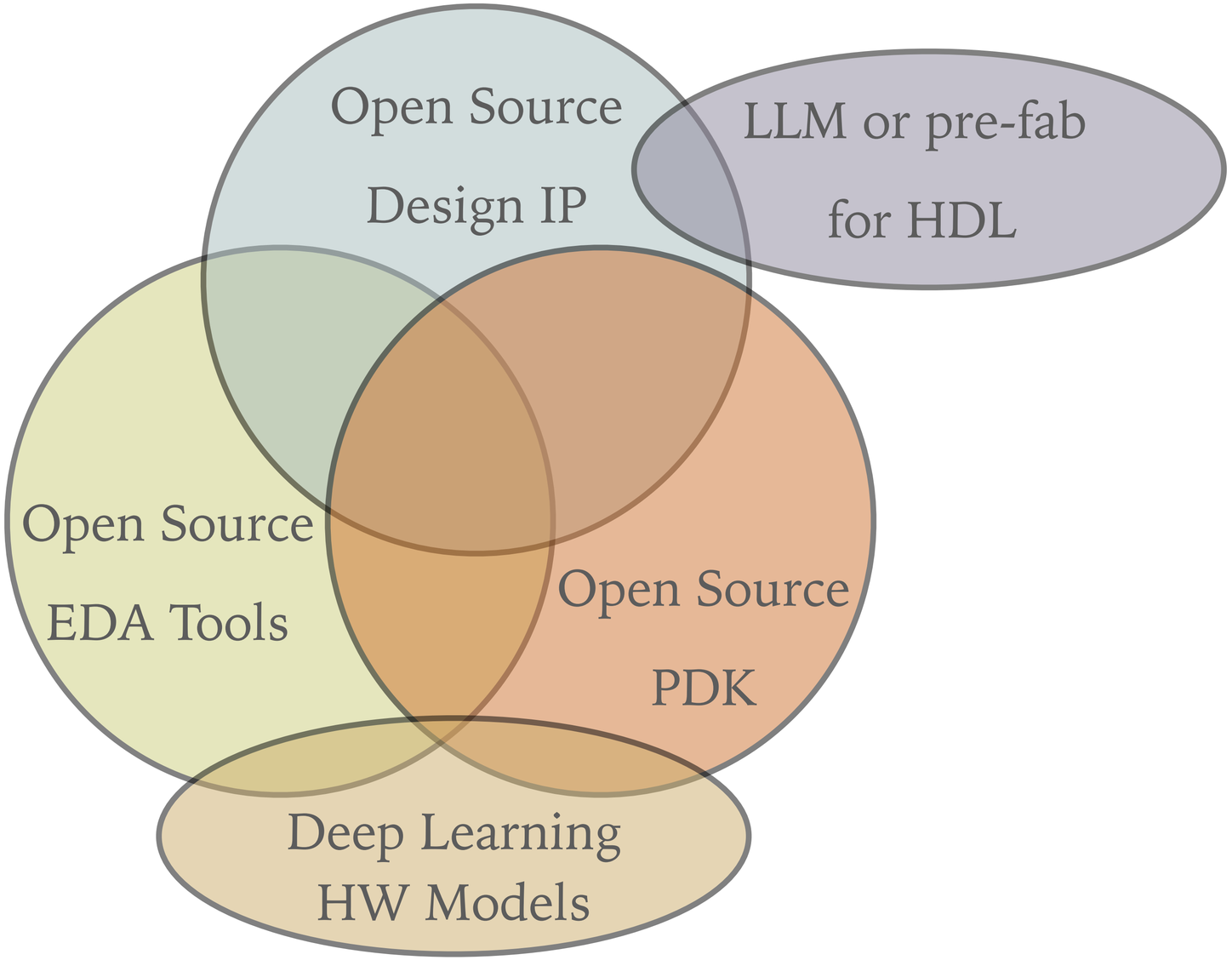
RECOMMENDATIONS FROM AND FOR EUROPE

- "Recommendations and Roadmap for Open-Source EDA in Europe" from the FOSSi Foundation. This document can be found here: https://fossi-foundation.org/resources/eu-roadmap
- Technical: Open Source Analog and Mixed-Signal Designs, Interoperability and Verification, System on Chip
- Non-Technical: Open Source Licensed Output (OSI), Funding Access, Sustainability of Projects, Funding of Tapeouts, Industry Training and Academic Education, Conferences and Collaboration

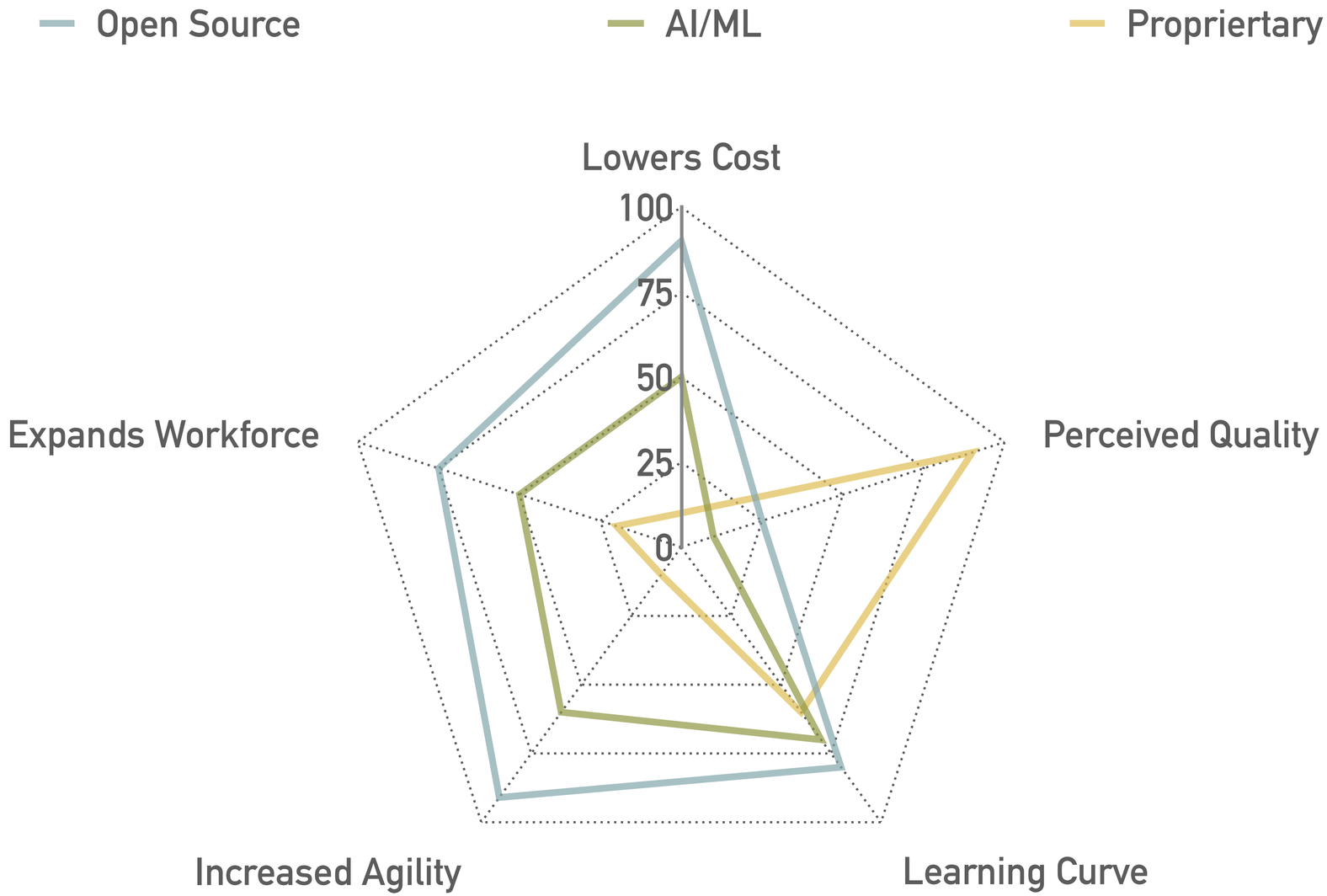
AREAS OF OPEN SOURCE SILICON DESIGN



AREAS OF OPEN SOURCE SILICON DESIGN – AI/ML



OPEN SOURCE AND AI/ML - OVERLAP AND OPPOSITION



SELECTED WORKS

- Large number of papers at https://ai4eda.github.io/
  - High level synthesis
  - Logic synthesis
  - Circuit verification
  - Floorplanning
  - Placement
  - Clock tree synthesis
  - Routing
  - Timing
  - Layout verification
  - Mask optimization
  - Testing
  - Dataset and tools

SELECTED WORKS (CONT)

- Papers at arXiv related to EDA
  - RTL Generation - A (very few) few examples -
    - RTLSquad: Multi-Agent Based Interpretable RTL Design
    - Accelerating Hardware Verification with Graph Models
    - MAGE: A Multi-Agent Engine for Automated RTL Code Generation
  - Design Verification -
    - UVLLM: An Automated Universal RTL Verification Framework using LLMs
    - CorrectBench: Automatic Testbench Generation with Functional Self-Correction using LLMs for HDL Design
    - FVEval: Understanding Language Model Capabilities in Formal Verification of Digital Hardware
  - High-Level Synthesis (HLS) -
    - Stream-HLS: Towards Automatic Dataflow Acceleration
    - HLSPilot: LLM-based High-Level Synthesis
  - Analog Design -
    - AnalogXpert: Automating Analog Topology Synthesis by Incorporating Circuit Design Expertise into Large Language Models

SELECTED WORKS (CONT)

- Papers at arXiv related to signal processing
  - Standards research
    - Chat3GPP: An Open-Source Retrieval-Augmented Generation Framework for 3GPP DocumentsAccelerating Hardware Verification with Graph Models
  - Coding
    - Detecting Convolutional Codes: A Markovian Approach with LRT and DNN
    - Successive Interference Cancellation-aided Diffusion Models for Joint Channel Estimation and Data Detection in Low Rank Channel Scenarios
  - Other
    - Large Language Model Agents for Radio Map Generation and Wireless Network Planning