Encoder Updates

18 October 2022

The problem

inline_config_adapter

The case switch for cfg (the enumerated tuple of frame type, constellation, and code rate) has some combinations that aren't in the tables in the spec. I volunteered to write a PR. Add DVB-S2X after DVB-S2 working.

DVB-S2 not working

We are not getting expected behavior with DMA => encoder => DAC FIFO path, using iio. The configuration word is getting corrupted, somehow, along the way, and causing a transmit buffer timeout in iio.

About that buffer...

iio_buffer_push()
iio_buffer_push_partial()

Partial is probably the right answer, because BBFrame lengths can vary. Sending single words to buffers works, sending files *usually* doesn't. Help needed.

Additional Capabilities

MQTT

Evariste and Anshul

Working on Pluto, not working on zc706. Will be a fantastic way to control a powerful radio.

Python Notebook

ts2bbframes.ipynb

Paul wrote a notebook that matches the block in GNU Radio that produces BBFrames from a TS file. It's in the tools directory in the integration repo.

PS Side improved

bitfile-to-PS workflow

We're now operating the station with iio calls on the processing side and have the workflow to go from nothing to DMA access documented in Working with FPGAs (documents).

Resources and Reaching Out

People

Sasha and Janani

Please welcome Sasha and Janani to the FPGA team. Look for them and make them welcome.

Community Support

Ham Expo, JAMSAT

Strong support for the project from Ham Expo and successful presentations to JAMSAT. Thank you to everyone helping to get out the word.

articles

Follow-up to OPV

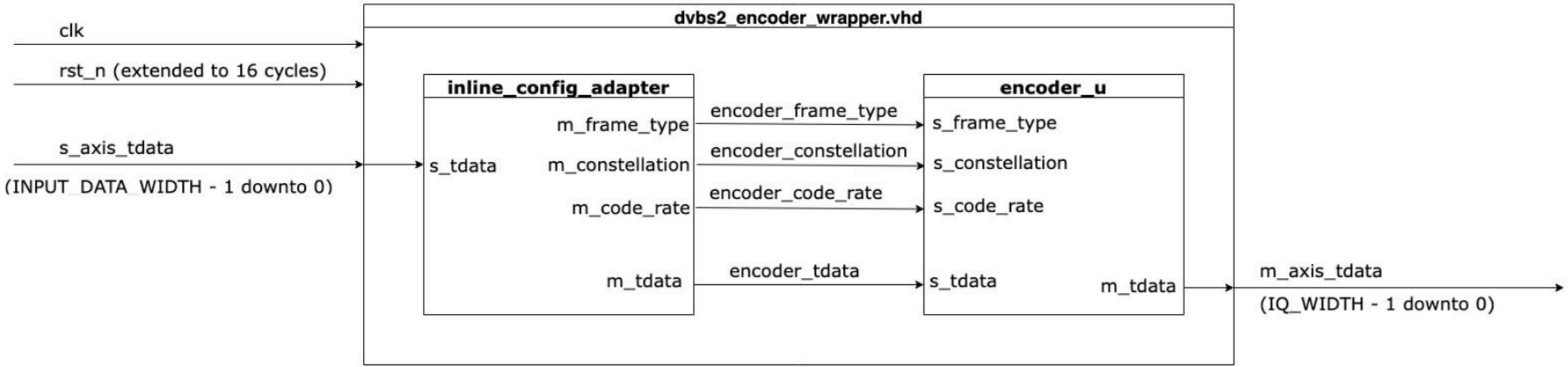
With an article about Opulent Voice likely to be published soon, we need to follow that up with one about multiplexing and the encoder.

Explanation Diagrams for Phase 4 Downlink

https://github.com/phase4ground/dvb_fpga/blob/master/build/vivado/dvbs2_encoder_wrapper.vhd

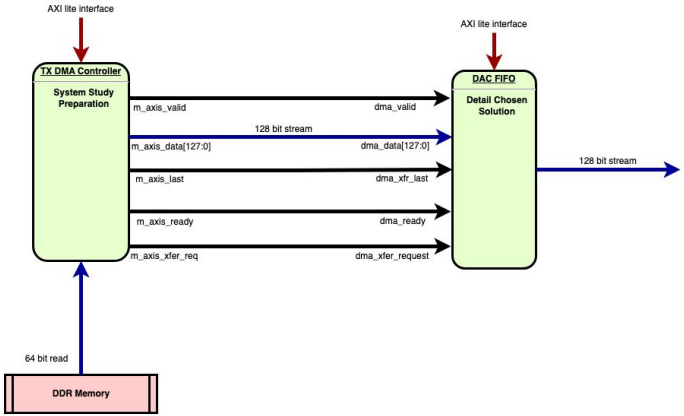
Thu Oct 13 2022

Things we
INPUT_DAT
IQ_WIDTH
AXI lite int



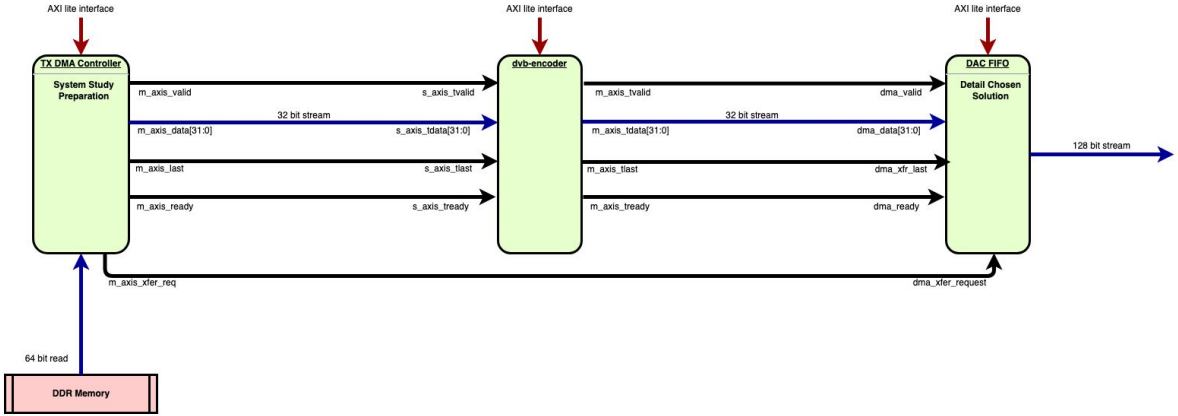
DVB-S2 Encoder Wrapper - what is placed in the HDL

Going inside the top block to look at the encoder itself, this is what the ports look like.



Encoder Integration

Above is the section of the ADI reference design as it is built from the ADI repository. Below is the encoder integrated into the reference design. The bus widths have to be adjusted for the encoder as it is written today.



Encoder is in between the TX DMA controller and the DAC FIFO.

We adjusted the bus widths (again) for the input side but still have a mismatch on the output side.