RISC-V®

Instruction Sets Want to be Free of Gravity!

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SiFive Inc.

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Why Instruction Set Architecture matters

- **Why can't Intel sell mobile chips?**
  - 99%+ of mobile phones/tablets based on ARM v7/v8 ISA
- **Why can't ARM partners sell servers?**
  - 99%+ of servers based on AMD64 ISA (most built by Intel)
- **How can IBM still sell mainframes?**
  - IBM 360, oldest surviving ISA (50+ years)

ISA is most important interface in computer system

where software meets hardware

Companies and their ISAs Come and Go

- Digital Equipment Corporation, RIP! (**PDP-11**, **VAX**, **Alpha**)
- Intel's dead ISAs (**i960**, **i860**, **Itanium, …**)
- **SPARC**
  - Sun opened v8 as IEEE 1754-1994
  - Acquired by Oracle, SPARC development closed down in 2017
- **MIPS**
  - Sold to Imagination, bought by Wave
  - Opened up MIPS R6 ISA in 2018, then made ***not*** open in 2019
- **IBM POWER**
  - Initially proprietary, opened up in 2019 as OpenPower
- **ARM**
  - Sold to Softbank in 2016
  - In 2020, Nvidia announced acquiring ARM

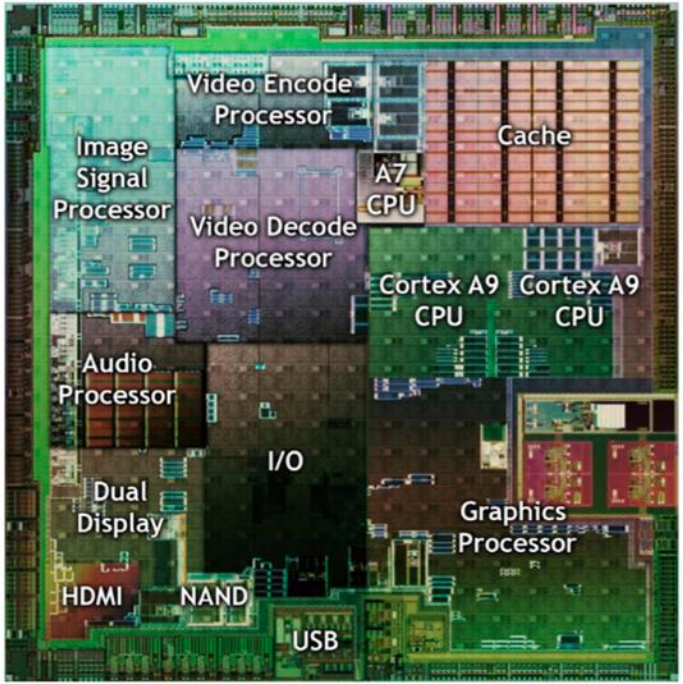
Open Interfaces Work for Software!

Field	*Open Standard*	*Free, Open Implement.*	*Proprietary Implement.*
Networking	Ethernet, TCP/IP	Many	Many
OS	Posix	Linux, FreeBSD	M/S Windows
Compilers	C	gcc, LLVM	Intel icc, ARMcc
Databases	SQL	MySQL, PostgresSQL	Oracle 12C, M/S DB2
Graphics	OpenGL	Mesa3D	M/S DirectX
ISA	??????	----------	x86, ARM, IBM360

- Why not successful free & open standards and free & open implementations, like other fields?

Today, many ISAs on one SoC

- Applications processor (usually ARM)
- Graphics processors
- Image processors
- Radio DSPs
- Audio DSPs
- Security processors
- Power-management processor
- *> dozen ISAs on some SoCs – each with unique software stack*



NVIDIA Tegra SoC

Why?

- Apps processor ISA too big, inflexible for accelerators
- IP bought from different places, each proprietary ISA
- Engineers build home-grown ISA cores

Do we need all these different ISAs?

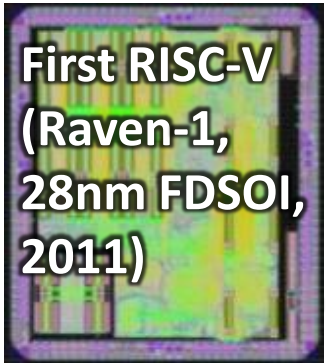
Must they be proprietary?

Must they keep disappearing?

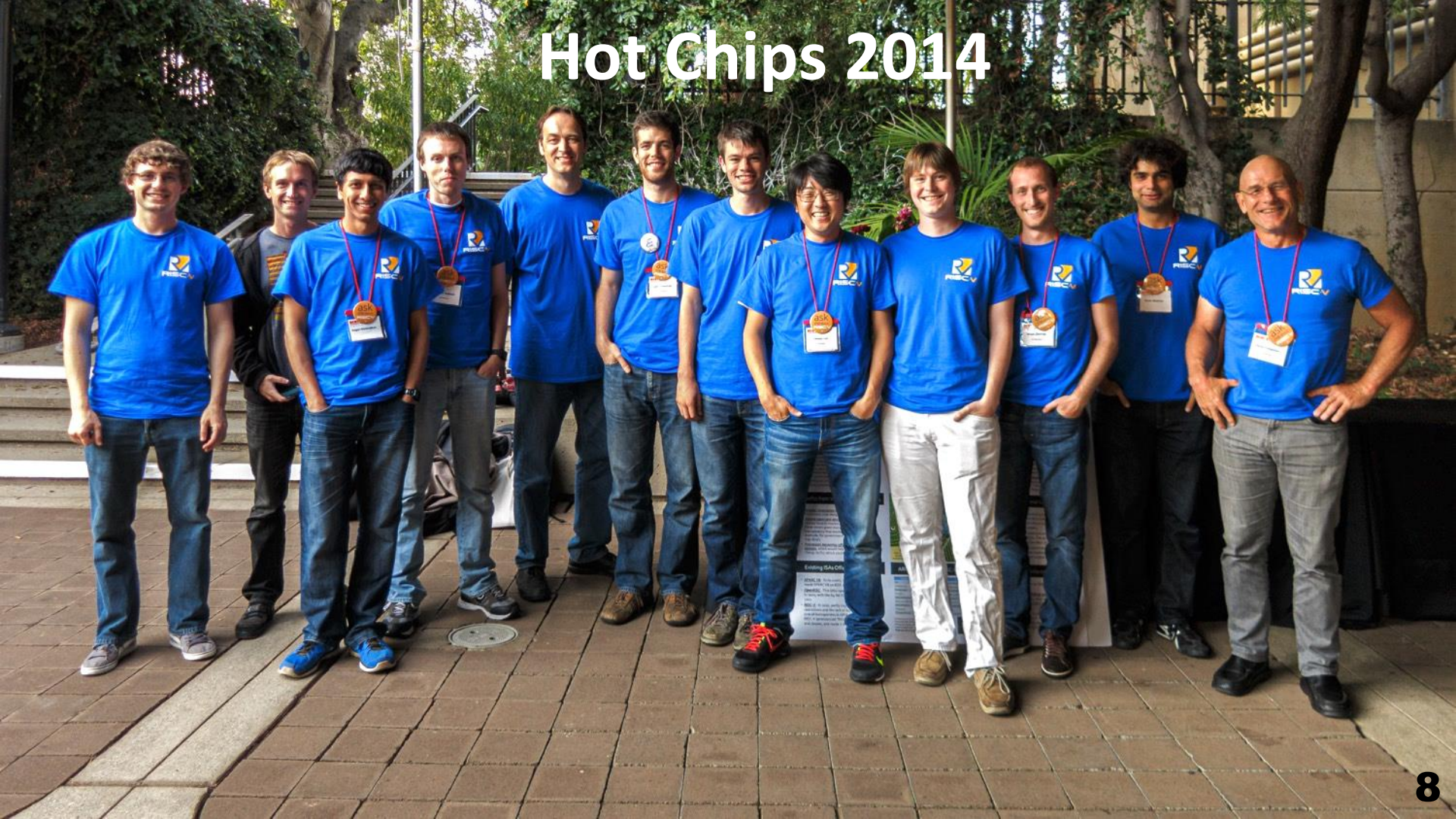
What if there was one stable free and open ISA everyone could use for everything?

RISC-V Background

- In 2010, after many years and many research projects using MIPS, SPARC, and x86, time for architecture group at UC Berkeley to choose ISA for next set of projects
- Obvious choices: x86 and ARM
  - x86 impossible – too complex, IP issues
  - ARM mostly impossible – complex, no 64-bit in 2010, IP issues
- So we started "3-month project" during summer 2010 to develop clean-slate ISA
  - Principal designers: Andrew Waterman, Yunsup Lee, David Patterson, Krste Asanovic
- Four years later, May 2014, released frozen base user spec
  - many tapeouts and several research publications along the way
- Name RISC-V (pronounced "risk-five") represents fifth major Berkeley RISC ISA



Hot Chips 2014



RISC-V is not first open ISA

- MIL-STD-1750A
  - Previous open military ISA defined by US Air Force, deprecated for new designs in 1996
- SPARC International
  - SPARC v8 IEEE standard, used by LEON for European Space Agency
- OpenRISC
  - Some uptake but project languishing in 2010, focused on core not ISA

- RISC-V has far broader acceptance and uptake than any of these

RISC-V International

- **RISC-V** is the open-source hardware Instruction Set Architecture (ISA)
- Frozen base user spec released in 2014, contributed, ratified, and openly published by RISC-V International

RISC-V International is a non-profit entity serving members and the industry

Our mission is to accelerate RISC-V adoption with shared benefit to the entire community of stakeholders.

- ✓ Drive progression of **ratified specs, compliance suite, and other technical deliverables**
- ✓ **Grow the overall ecosystem / membership**, promoting diversity while preventing fragmentation
- ✓ Deepen **community engagement and visibility**

RISC-V Ecosystem

Software

Open-source software:
Gcc, binutils, glibc, Linux, BSD, LLVM, QEMU, FreeRTOS, ZephyrOS, LiteOS, SylixOS, …

Commercial software:
Lauterbach, Segger, IAR, Micrium, ExpressLogic, Ashling, Imperas, AntMicro, …

RISC-V International

ISA specification | Golden Model | Compliance

Hardware

Open-source cores:
Rocket, BOOM, RI5CY, Ariane, PicoRV32, Piccolo, SCR1, Swerv, Hummingbird, WARP-V, XiangShan, …

Commercial core providers:
Alibaba, Andes, Bluespec, Cloudbear, Cobham, Codasip, Cortus, InCore, MIPS, Nuclei, Semidynamics, SiFive, StarFive, Syntacore, …

Inhouse cores:
Nvidia, WDC, Alibaba, +others

What's Different about RISC-V?

- *Simple*
  - Far smaller than other commercial ISAs
- *Clean-slate design*
  - Clear separation between user and privileged ISA
  - Avoids µarchitecture or technology-dependent features
- *Modular* ISA designed for *extensibility/specialization*
  - Small standard base ISA, with multiple standard extensions
  - Sparse &variable-length instruction encoding for vast opcode space
- *Stable*
  - Base and first standard extensions are frozen
  - Additions via optional extensions, not new versions
- *Community designed*
  - Developed with leading industry/academic experts and software developers

Engaged engineers are domain experts

Drive technical priorities in 20+ focus areas

Compliance

Technical Deliverables

Opcode Space Mgmt Standing Committee

Software Standing Committee

Base ISA Ratification Task Group

Privileged ISA Spec Task Group

UNIX-Class Platform Spec Task Group

Formal Specification Task Group

Trusted Execution Env Spec Task Group

B Extension (Bit Manipulation) Task Group

J Extension (Dynam. Translated Lang) Task Group

P Extension (Packed-SIMD Inst) Task Group

V Extension (Vector Ops) Task Group

Cryptographic Extension Task Group

Debug Specification Task Group

Fast Interrupts Spec Task Group

Memory Model Spec Task Group

Processor Trace Spec Task Group

Compliance Task Group

+ Security Committee, HPC Special interest group, soft-core SIG, and Safety Task Group

Our Modest RISC-V Project Goal

Become the industry-standard ISA for all computing devices

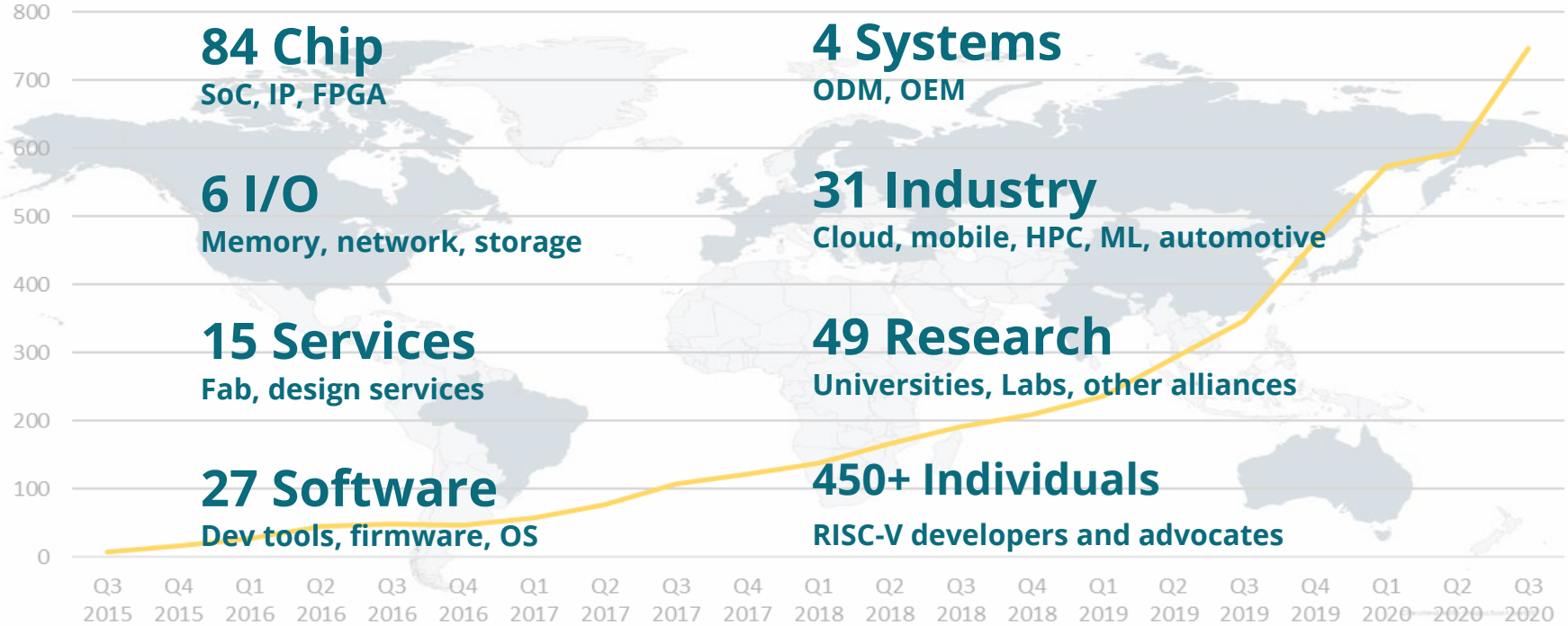
This is happening!

Far faster, more domains, than anyone predicted
Demand at every performance level (low to ludicrous)
Demand for all features of all other ISAs ever built!

Using a new community ISA spec development model

More than 750 RISC-V Members

across 50 Countries



84 Chip
SoC, IP, FPGA

4 Systems
ODM, OEM

6 I/O
Memory, network, storage

31 Industry
Cloud, mobile, HPC, ML, automotive

15 Services
Fab, design services

49 Research
Universities, Labs, other alliances

27 Software
Dev tools, firmware, OS

450+ Individuals
RISC-V developers and advocates

So far in 2020, RISC-V membership has grown by more than 50%


Aril Inc
astc
antmicro
aselsan
Allwinner
Alibaba.com
AdaCore
adafruit
Airavath Foundation
APEXMIC
GRADIENT
ASHLING
AIST
Barcelona Supercomputing Center
Baylibre
Berkeley Architecture Research
BITMAN
bluespec
创景科技
BOSTON UNIVERSITY
BAE SYSTEMS
सी डैक CDAC
cadence
Cancun
cortus
सी डैक CDAC एक्सटस acts
Authorized Training Centre
cea
Centipede
CEVA
CLEMSON
CloudBEAR
COBHAM
DATA 61
csem
codasip
Collins Aerospace
CRYPTAPE
CPSEC
DOVER MICROSYSTEMS
RISC-V
DRAPER
dxcorr
EMBECOSM
EMDALO TECHNOLOGIES
Esperanto TECHNOLOGIES
ESPRESSIF
ETH zürich
expresslogic
oculus
FORTH
FOUNDRISCO
galois
GENESYS
GHELIA
GigaDevice
GOLDEN GATE UNIVERSITY
Google
GOWIN
GREENWAVES
TU Graz
HENSOLDT
Hewlett Packard Enterprise
HEX-Five Security
HIGO 海芯
HITACHI Inspire the Next
Honeywell
HORTONWORKS
HUAWEI
huami
IAR SYSTEMS
IBM
ICT
IDT Integrated Device Technology
Imagination
imperas
imt.
infineon
君正 Ingenic
Inria
inside secure
inspur 浪潮
ISCAS
INTRINSIC ID
Intrinsix
jumptrading
KU LEUVEN
LATTICE
LAUTERBACH DEVELOPMENT TOOLS
lowRISC
MEDIATEK
Mellanox
Mentor A Siemens Business
MICROCHIP
MIT CSAIL
Microsemi Power Matters.
MOSIS
MINRES TECHNOLOGIES
Micron
Morse Micro
Mosaik
Minima
NSI-TEXE
芯来科技 NUCLEI
NVIDIA
NUS National University of Singapore
NOKIA
NORDIC SEMICONDUCTOR
Ockam
onespin
OPENHW
ORION 猎户星空
pango
PerfXLab 澎峰科技
Pacific Northwest NATIONAL LABORATORY
PRINCETON UNIVERSITY
PEZY Computing
qamcom
QUALCOMM
QuickLogic
Rambus
Rumble Development
NERVOS
NETRONOME
NORTHROP GRUMMAN
NXP
SEMIDRIVE
SECURE RF
SEAGATE
SANECHIPS 中兴微电子
SAMSUNG
SEGGER
semidynamics
SiFive
SIEMENS
SILICON LABS
SK hynix
SHC SH CONSULTING
SONY
SoundAI
sparkfun ELECTRONICS
SILEX INSIGHT
Roa Logic
REM
Red Hat
SRI International
surecore
Symbiotic EDA
Syntacore
Syntronix
Semiconductor Investment
SYZEXION
Tactical Computing Labs
TANGRAM
TechanaLye
Technolution
Telink
KTrustKernel 上海瓶钵信息科技有限公司
THALES
TIMESILICON
Tortuga Logic
TRINAMIC
tsmc
Think Silicon
UEC The University of Electro-Communications
UBILITE
优砂科技 UC TECH IP
ultra soc
云知声 Unisound
Universidade do Minho
東京大学 THE UNIVERSITY OF TOKYO
University of BRISTOL
UPPSALA UNIVERSITET
KU
VectorBlox
VeriSilicon
创景科技
Western Digital
WIND RIVER
WIT
潍柴动力 WEICHAI POWER
XILINX
XtremeEDA
ZeroPoint
信大捷安

CHINA

MORE THAN 200 MEMBERS HAVE JOINED THE CRVA AND CRVIC ASSOCIATIONS AS WELL AS 33 MEMBERS IN THE GLOBAL RISC-V FOUNDATION. ACROSS 2019 WE'VE LED DISCUSSIONS IN 6 CITIES AS WELL AS HOSTED A DAY OF TALKS AT THE WORLD INTERNET CONFERENCE. IN NOVEMBER, WE HOSTED 500 ATTENDEES AT THE CHINA RISC-V FORUM.

EUROPE

THE EUROPEAN PROCESSOR INITIATIVE HAS DECLARED RISC-V AS A KEY ARCHITECTURE FOR THE NEXT GENERATION OF HPC PROCESSORS AND SYSTEMS, FOCUSED ON ACCELERATION.

INDIA

2014 WITH THE FUNDING OF 6 RISC-V PROCESSORS THROUGH THE SHAKTI PROJECT, RISC-V HAS BEEN WIDELY DECLARED THE NATIONAL ARCHITECTURE OF INDIA.

JAPAN

MOMENTUM IS CONTINUING TO GROW IN OUR ENGAGEMENT AND EVENTS WITH A 50% JUMP AT OUR 2019 TOKYO DAY TO 360 REGISTERED ATTENDEES.

PAKISTAN

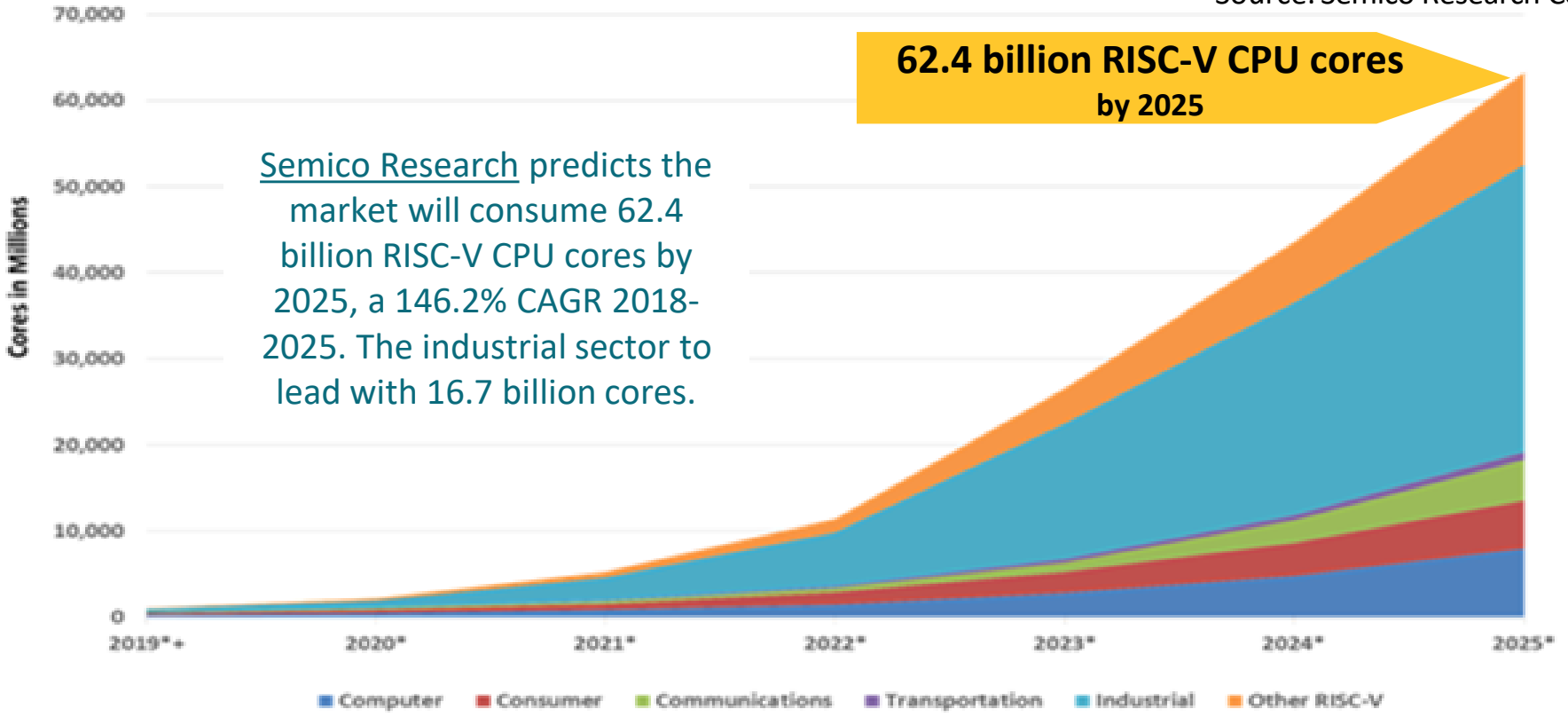
ON THE ROAD TO DECLARING RISC-V THEIR NATIONAL ARCHITECTURE, TWO OF THE BIGGEST GATHERINGS EVER OF 3000+ IN PAKISTAN FOR TWO SIFIVE TECH SYMPOSIUMS – OCT 2019

NORTH AMERICA

NORTH AMERICA. INDUSTRY ADOPTION HAS TAKEN OFF WITH MILLIONS OF CORES SHIPPING FROM NVIDIA, WESTERN DIGITAL, SIFIVE, AND OTHERS.

Rapid RISC-V growth over next five years led by industrial

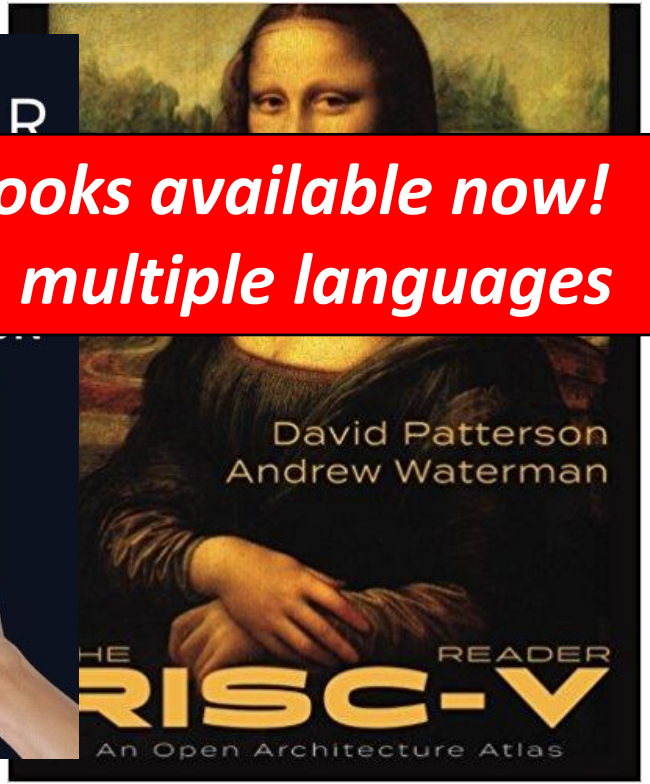
Source: Semico Research Corp



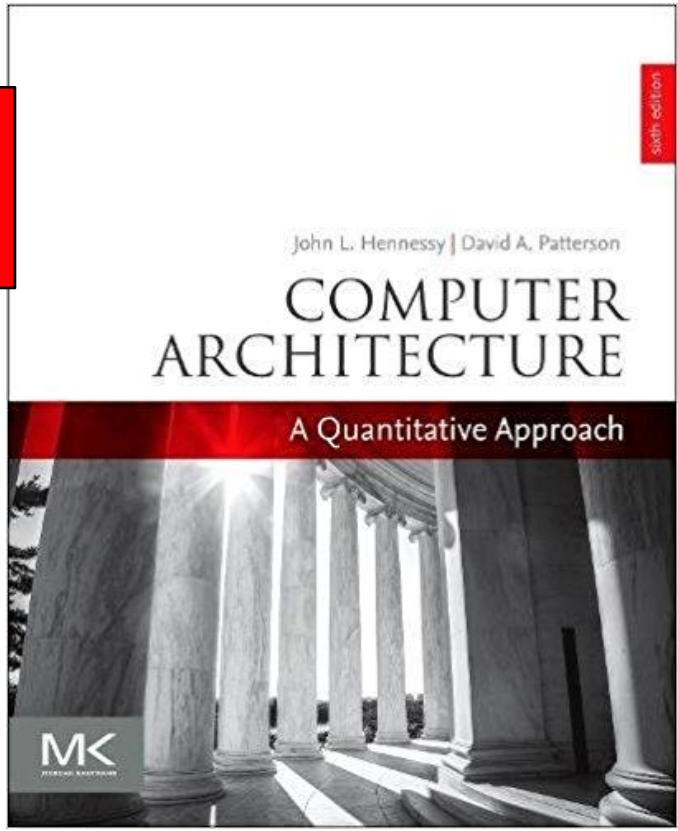
Why is RISC-V so popular?

- Engineers sometimes "*don't see forest for the trees*"
- The movement is ***not*** happening because some benchmark ran 10% faster, or some implementation was 30% lower power
- The movement ***is*** happening because ***new business model*** changes everything
  - Pick ISA first, then pick vendor or build own core
  - Add your own extension without getting permission
- Implementation features/PPA will follow
  - Whatever is broken/missing in RISC-V will get fixed

RISC-V in Education



Books available now!
In multiple languages



RISC-V spreading quickly throughout curricula of top schools

RISC-V for Space Computing

- Simple
- Extensible
- Stable
- Secure

RISC-V Simplicity

- Small base, but sufficient to run full C compiler and software stack with good efficiency
- Provides minimal “skeleton” on which to hang additional standard or custom extensions

- Shallow learning curve
- Reduced gate count for small implementations
- Reduced verification cost
- Ease ramp for implementation teams
- Reduce effort for fault-tolerant designs

RV32I Base Unprivileged Instructions

imm[31:12]			rd	0110111	LUI
imm[31:12]			rd	0010111	AUIPC
imm[20|10:1|11|19:12]			rd	1101111	JAL
imm[11:0]	rs1	000	rd	1100111	JALR
imm[12|10:5]	rs2	rs1	000	imm[4:1|11]	1100011	BEQ
imm[12|10:5]	rs2	rs1	001	imm[4:1|11]	1100011	BNE
imm[12|10:5]	rs2	rs1	100	imm[4:1|11]	1100011	BLT
imm[12|10:5]	rs2	rs1	101	imm[4:1|11]	1100011	BGE
imm[12|10:5]	rs2	rs1	110	imm[4:1|11]	1100011	BLTU
imm[12|10:5]	rs2	rs1	111	imm[4:1|11]	1100011	BGEU
imm[11:0]		rs1	000	rd	0000011	LB
imm[11:0]		rs1	001	rd	0000011	LH
imm[11:0]		rs1	010	rd	0000011	LW
imm[11:0]		rs1	100	rd	0000011	LBU
imm[11:0]		rs1	101	rd	0000011	LHU
imm[11:5]	rs2	rs1	000	imm[4:0]	0100011	SB
imm[11:5]	rs2	rs1	001	imm[4:0]	0100011	SH
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	SW
imm[11:0]		rs1	000	rd	0010011	ADDI
imm[11:0]		rs1	010	rd	0010011	SLTI
imm[11:0]		rs1	011	rd	0010011	SLTIU
imm[11:0]		rs1	100	rd	0010011	XORI
imm[11:0]		rs1	110	rd	0010011	ORI
imm[11:0]		rs1	111	rd	0010011	ANDI
0000000	shamt	rs1	001	rd	0010011	SLLI
0000000	shamt	rs1	101	rd	0010011	SRLI
0100000	shamt	rs1	101	rd	0010011	SRAI
0000000	rs2	rs1	000	rd	0110011	ADD
0100000	rs2	rs1	000	rd	0110011	SUB
0000000	rs2	rs1	001	rd	0110011	SLL
0000000	rs2	rs1	010	rd	0110011	SLT
0000000	rs2	rs1	011	rd	0110011	SLTU
0000000	rs2	rs1	100	rd	0110011	XOR
0000000	rs2	rs1	101	rd	0110011	SRL
0100000	rs2	rs1	101	rd	0110011	SRA
0000000	rs2	rs1	110	rd	0110011	OR
0000000	rs2	rs1	111	rd	0110011	AND
fm | pred | succ		rs1	000	rd	0001111	FENCE
000000000000		00000	000	00000	1110011	ECALL
000000000001		00000	000	00000	1110011	EBREAK

RISC-V Base Plus Standard Extensions

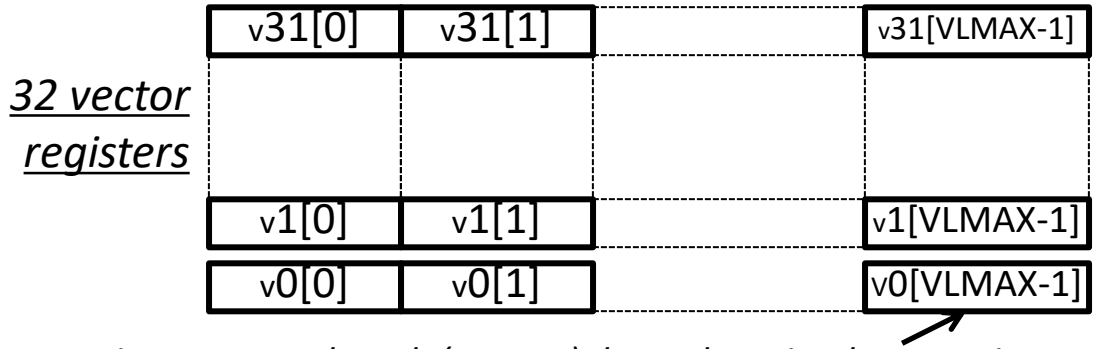
- Four base integer ISAs
  - RV32E, RV32I, RV64I, RV128I
  - RV32E is 16-register subset of RV32I
  - Only <50 hardware instructions needed for base
- Standard extensions
  - M: Integer multiply/divide
  - A: Atomic memory operations (AMOs + LR/SC)
  - F: Single-precision floating-point
  - D: Double-precision floating-point
  - G = IMAFD, “General-purpose” ISA
  - Q: Quad-precision floating-point
- Above use standard RISC encoding in fixed 32-bit instruction word
- Frozen in 2014, ratified 2019, supported forever after

RISC-V Extensibility

- RISC-V originally designed for research into application-specific processors
- Small base with supported compiler reduces incentive to design new base for each type of core
- No “permission” needed to build your own custom extension

- RISC-V being used in many AI/ML accelerator projects

RISC-V Vector Extension (RVV) Overview



Maximum vector length (VLMAX) depends on implementation, number of vector registers used, and type of each element.

- Unit-stride, strided, scatter-gather, structure load/store instructions
- Rich set of integer, fixed-point, and floating-point instructions
- Vector-vector, vector-scalar, and vector-immediate instructions
- Multiple vector registers can be combined to form longer vectors to reduce instruction bandwidth or support mixed-precision operations (e.g., 16b*16b->32b multiply-accumulate)
- Designed for extension with custom datatypes and widths

Vector CSRs

vtype

Vtype sets width of element in each vector register (e.g., 16-bit, 32-bit, …)

vl

Vector length CSR sets number of elements active in each instruction

vstart

Resumption element after trap

vcsr (vxrm/vxsat)

Fixed-point rounding mode and saturation flag fields in vector CSR

Some RVV Design Points

Name	Issue Policy	Issue Width	VLEN (bits)	Datapath (bits)	VLEN/Datapath (beats)
Smallest	InO	1	32	32	1
Simple	InO	1	512	128	4
InO-Spatial	InO	2	128	128	1
OoO-Spatial	OoO	2-3	128	128	1
OoO-Temporal	OoO	2-3	512	128	4
OoO-Server	OoO	3-6	2048	512	4
OoO-HPC	OoO	3-6	16384	2048	8

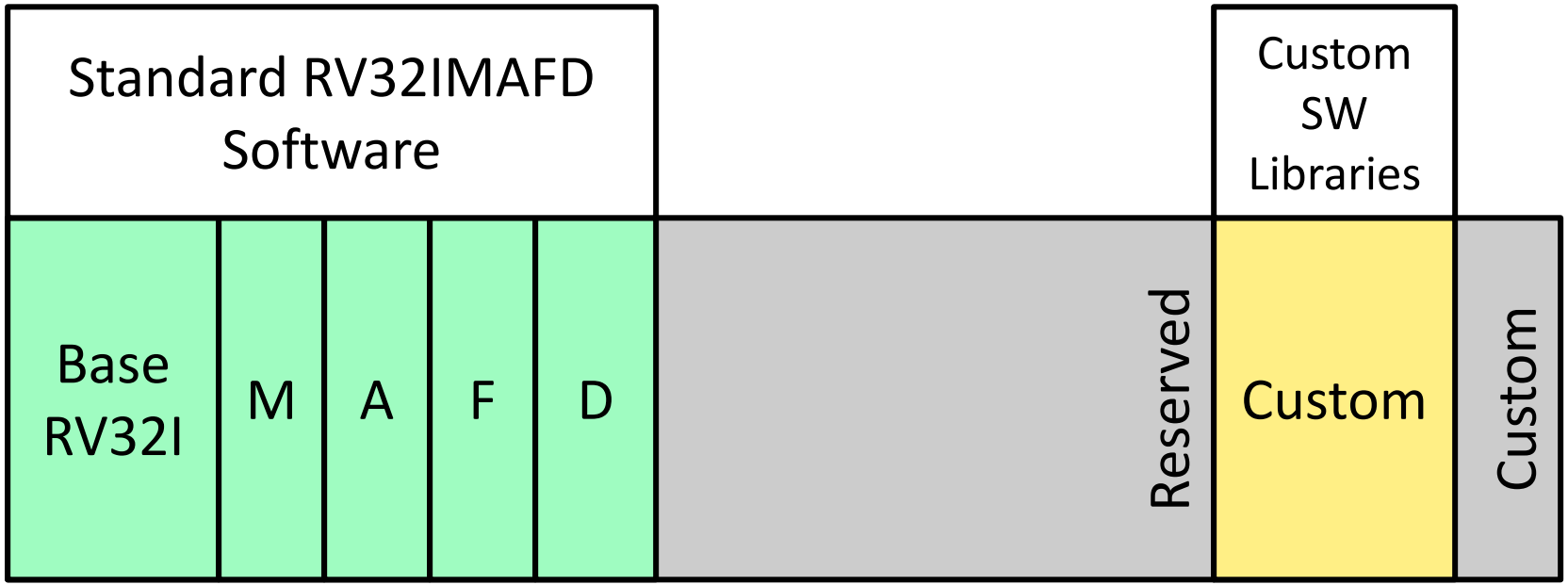
RISC-V Encoding Terminology

Standard: defined by RISC-V

Reserved: RISC-V might eventually use this space for future standard extensions

Custom: Space for implementer-specific extensions, never claimed by RISC-V

RISC-V Custom Extension Example



Fragmentation versus Diversity

Fragmentation:
Same thing done different ways

Diversity:
Solving different problems

How is RISC-V Avoiding Fragmentation?

Two powerful forces keep fragmentation at bay:

- **Users**: No one wants a repeat of vendor lock-in.
- **Software**: No one, not even nation state, can afford their own software stack. Upstream open-source projects only accept frozen/ratified Foundation standards.

RISC-V Stability

- Designed around small base with modular extensions
- Extensions are frozen and don't change after ratification
- New features via new extensions
- No commercial incentive to force mandatory ISA upgrades
- ISA won't disappear due to merger/acquisition/liquidation
- Original base design will continue to be supported indefinitely

- *In 50th year of a mission, original RISC-V ISA should still be supported with standard software tools*

RISC-V Security

- Original ISA designed with security in mind
- Reduced formal verification effort due to simplicity
- Open ISA design encourages research/inspection
  - RISC-V has become focus of secure architecture research community

RISC-V for Space Computing

- Stable, simple, efficient, flexible, secure, open ISA
- Expressly designed to support custom use cases
- Strong and rapidly growing open-source hardware and software ecosystem
- Strong and rapidly growing commercially supported hardware and software ecosystem
- Leading choice for new designs for AI/ML and security