System Design Document

SatNOGS COMMS

Libre Space Foundation

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DRAFT

Contents

1. Introduction

1.1 Purpose

The purpose of this document is to effectively define the SatNOGS COMMS system architecture and design, and give clear guidance to the team implementing the system. The document is produced incrementally and iteratively during the system development life-cycle.

1.2 Intended audience

The intended audiences of this document are developers who will implement the SatNOGS COMMS solution as well as the European Space Agency and the entities that have signed the Letter of Interest for this development (the latter on an informational capacity). It is assumed that the reader is familiar with satellite communications in general and more specifically, satellite communication subsystems, both for space and ground segments. It is also assumed that the reader has some knowledge of radio communications technologies, as well as modulation and decoding schemes and basic knowledge of electronics design.

1.3 Scope

The scope of this system Design Document is the development of SatNOGS COMMS. SatNOGS COMMS is a versatile telecommunications solution suitable for nano-satellites and Cubesats, operating in UHF and S-band, and featuring tight integration with SatNOGS network. The scope spans from the space segment transceiver to the ground segment station.

1.4 Acronyms

ADC Analog to Digital Converter

AGC Automatic Gain Control

API Application programming interface

balun Balanced to Unbalanced

BER Bit Error Rate

BOM Bill of Materials

BPF Band Pass Filter

BPSK Binary Phase Shift Keying

CAN Controller Area Network

CANFD Controller Area Network flexible data-rate

CCSDS Consultative Committee for Space Data Systems

CIC Cascaded integrator–comb filter

COTS Commercial off the Self

CRC Cyclic Redundancy Check

DAC Digital to Analog Converter

DSP Digital Signal Processing

DSSS Direct Sequence Spread Spectrum

ECC Error-correcting code

EDV Energy Detection Value

EIRP Effective isotropically radiated power

EMI Electromagnetic Interference

eMMC embedded Multi-Media Controller

ENOB Effective number of bits

FEC Forward Error Correction

FER Frame Error Rate

FPGA Field Programmable Gate Array

FSK Frequency Shift Keying

gRPC gRPC Remote Procedure Calls

HAL Hardware Abstraction Layer

HDF5 Hierarchical Data Format

I2C Inter-Integrated Circuit

IC Integrated Circuit

IF Intermediate Frequency

IO Input/Output

IP3 Third-order intercept point

ISM Industrial, Scientific and Medical

LEO Low Earth Orbit

LNA Low Noise Amplifier

LO Local Oscillator

LVDS Low Voltage Differential Signaling

MCU Micro-Controller Unit

MDS Minimum Detectable Signal

MSK Minimum Shift Keying

MSPS Mega Samples per Symbol

NF Noise Figure

OSDLP Open Space Data Link Protocol

OTP One time programmable

PA Power Amplifier

PAPR Peak to Average Power Ratio

PCB Printed Circuit Board

PMIC Power management integrated circuits

QA Quallity Assurance

QPSK Quadrature Phase Shift Keying

RF Radio Frequency

RPC Remote Procedure Calls

RSSI Received signal strength indication

RX Receive

SAW Surface acoustic wave

SBC Single Board Computer

SDR Software Defined Radio

SEU Single-event upset

SFD Start Frame Delimiter

SNR Signal-to-noise ratio

SPI Serial Peripheral Interface

SQNR Signal-to-quantization-noise ratio

TC&C Tele-command & Control

TCXO Temperature compensated crystal oscillator

TLE Two Line Element

TMR Triple Mode Redundancy

TMTC Telemetry & Tele-control

TX Transmit

UHF Ultra High Frequency

VGA Variable Gain Amplifier

VPL Visual Programming Language

2. Overview

The SatNOGS COMMS is a turnkey solution enabling robust and reliable communication for LEO Cubesats. It operates in the UHF and S frequency bands, providing uplink and downlink capabilities on both of these spectrum regions. Demodulation and decoding of telemetry and payload data produced by SatNOGS COMMS is fully compatible with SatNOGS ground stations. SatNOGS COMMS also integrates tightly to SatNOGS Network, supporting a mission control system for TC&C and real-time dashboards. The SatNOGS COMMS architecture consists of two major modules, the space and the ground segment. The space segment consists of the hardware and the corresponding software that controls it, while the ground segment is used for uplink and downlink.

3. Architecture

3.1 Architectural Design

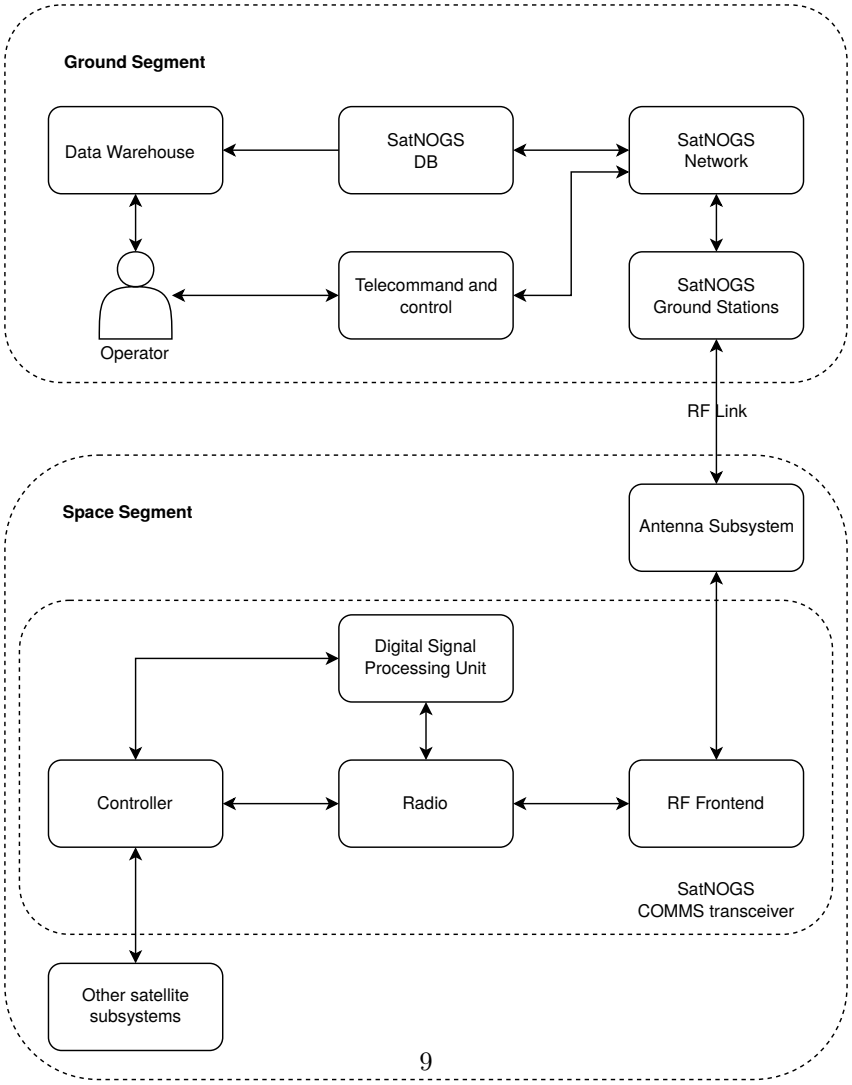

Figure 3.1: SatNOGS COMMS components

This section describes the architecture and system design of SatNOGS COMMS. Figure 3.1 depicts an abstraction of the SatNOGS COMMS key functional components.

On the space segment, the SatNOGS COMMS transceiver provides two half-duplex RF interfaces, operating independently in the UHF and S-Band respectively. The UHF interface operates in the 395–500 MHz frequency range for both TX and RX. For the S-Band interface, the COMMS transceiver utilizes the $\{[2200-2290],[2400-2450]\}$ MHz for TX and $\{[2025-2110],[2200-2290],[2400-2450]\}$ MHz for RX. The primary functions of the transceiver are modulation and coding following the CCSDS recommendations for Category A spacecrafts. The available framing schemes follow the IEEE 802.15.4 and CCSDS (user selectable), while the supported modulations are BPSK, QPSK, MSK, FSK. The COMMS transceiver provides an I/Q interface to extend the radio functionality (additional modulations, framing schemes) and enable Cognitive Radio capabilities (spectrum monitoring, collision avoidance, machine learning).

Two processing units assists the COMMS transceiver operation. An FPGA is responsible for the implementation of time critical and computationally intensive DSP operations, while a MCU orchestrates the functional components of the COMMS, providing also a communication interface with other subsystems of the spacecraft or the ground segment. Moreover, the SatNOGS COMMS transceiver provides two dedicated RF front-ends, one for each band of operation. Each of the RF front-ends, incorporates a PA for TX, band-pass filtering accompanied by an LNA for the RX and a high isolation RF switch that selects the proper signal path between the radio transceiver and the antenna port during TX/RX operations.

On the ground segment, the SatNOGS COMMS ground station is able to receive and transmit all the supported coding and modulation schemes of the COMMS transceiver. To achieve maximum flexibility, ground stations rely on the SDR technology. All the necessary DSP is performed entirely on software. Each SatNOGS COMMS ground station is fully integrated into the SatNOGS Network, extended with TC&C capabilities. In addition, SatNOGS provides the functions for mission control, telemetry storage and viewing through a set of visualization dashboards, configurable in a per customer and/or mission basis.

3.2 Decomposition Description

3.2.1 Hardware

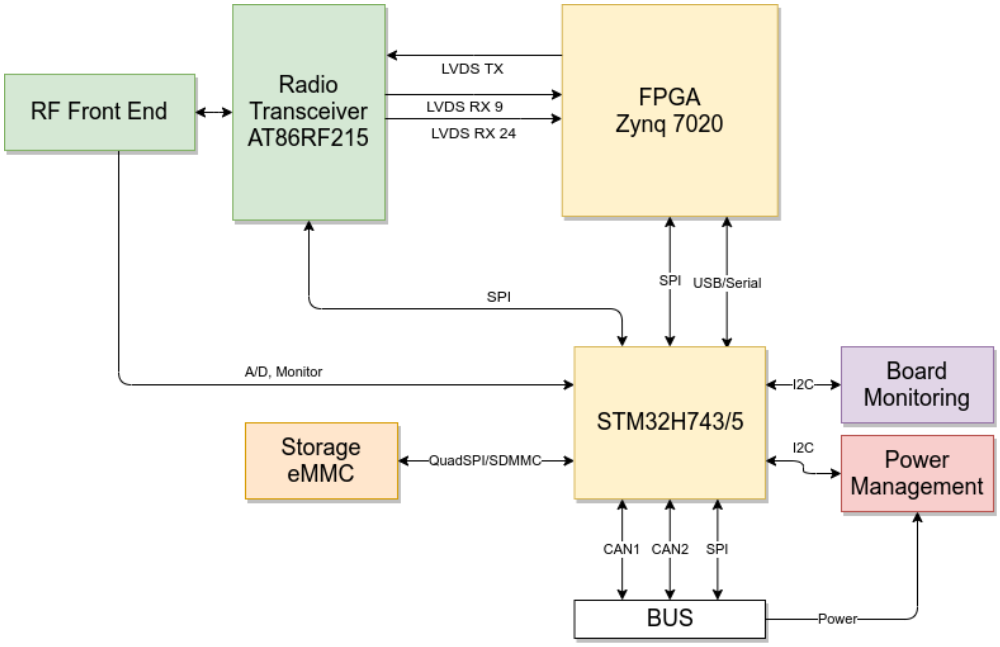

Figure 3.2: System blocks

RF Front End and Radio Transceiver

The SatNOGS COMMS board is based on the AT86RF215 [1] integrated circuit transceiver. This IC operates simultaneously on both UHF and 2.4 GHz ISM bands and supports all of the specified modulations. In addition, it provides an I/Q interface with a maximum sampling rate of 4 MSPS and a variety of user defined low pass filters. The DSP software of the SatNOGS COMMS transceiver utilizes this I/Q interface to implement the specified CCSDS modulation and coding schemes that are not available by the modem of the IC. Nevertheless, the integrated IEEE 802.15.4 hardware modem of the IC is still available.

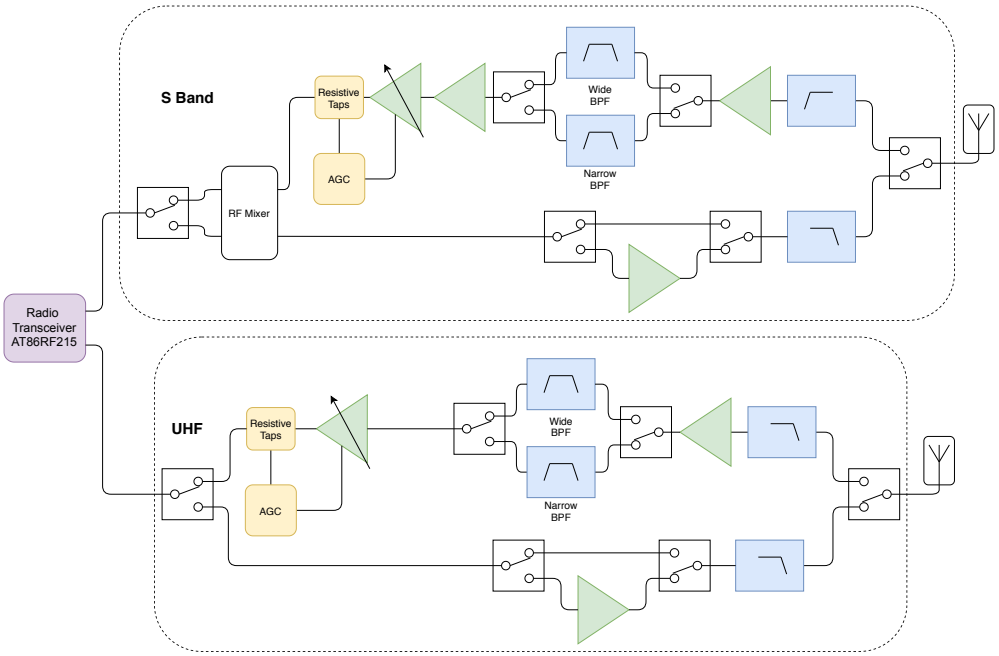

Figure 3.3: RF Front-End Architecture

Due to the limited tuning frequency range of the AT86RF215 IC in the S-band, the SatNOGS COMMS transceiver implements a walking-IF architecture. In this architecture scheme, a super-heterodyne radio is used along with an RF mixer. The RF mixer is placed between the antenna and the RF ports of the IC and it is responsible to either down- or up-convert the [2025–2110], [2200–2290], [2400–2450] MHz frequencies bands that are not covered by the tuning capabilities of the AT86RF215 IC, to an IF frequency region of [2366–2485] MHz. On the UHF band there is no need for an RF mixer, since the AT86RF215 supports the entire [399–500] MHz frequency range. To achieve concurrency, SatNOGS COMMS has a separate RF front-end for each band. A single antenna for each band is also available which is enough to satisfy the half-duplex communication requirements.

The S-band frontend is implemented to have a low noise figure in the RX chain, by using a series of band pass filters and LNAs. The goal is to maximize the selectivity without limiting the available dynamic range of the receiver and also prevent saturation, that will lead to intermodulation products in the presence of strong out of band signals. The TX function is designed to perform up to the specified output power and signal quality by using filters that reduce the harmonics, modulation and mixing artifacts.

To enable cognitive radio capabilities, each of the RX chains provide two different selectable signal paths. The first one is using a narrow band pass filter. This signal path is mostly suitable for normal operation, receiving and decoding frames originating

from ground station transmission at the coordinated frequency. At the second signal path, a wide band pass filter intervenes, enabling spectrum monitoring and congitive radio capabilities to be applied.

Controller

The controller unit is responsible for all unit coordination and control as well as subsystem communication. An MCU capable of providing processing power and necessary IO is chosen from the STM32H7 series. The selected MCU is the STM32F743 [2] having a maximum frequency of 460MHz, 2MB RAM, ECC memory and all required IO interfaces. There are ECC controllers for each RAM and flash bank that provide up to two errors detection and one error correction. Memory scrubbing will be performed on demand by software when errors occur. There are two watchdogs for supervising the MCU and handle lockups.

Digital Signal Processing Unit

The SatNOGS COMMS transceiver is equipped with ZYNQ-7020 FPGA[3] family. This FPGA is responsible for handling time critical DSP operations and communicate with the Serial I/Q Data Interface of the radio transceiver using an LVDS physical connection.

Storage

On-board storage unit is an eMMC memory module capable of covering the needs for store and forward functionality, COMMS firmware upgrade and multiple FPGA firmware for adaptive operations. Capacity can vary starting from 512MB depending on the application and is configurable during part selection and assembly.

Power supply

Power is supplied via two discrete DCDC converters for 3.3 and 5V and a fully programmable PMICs providing all the necessary voltage outputs needed by the FPGA. Low power RF circuits are powered by LDOs for minimal noise insertion. A PMIC was chosen due to is small footprint and power monitoring integration. PMIC offers voltage supervision by independent registers that disable output when an over-voltage occurs. Additionally, each PMIC output as well as DCDC outputs are monitored by hardware voltage supervisors that power-cycle COMMS by master MOSFET placed between BUS and DCDC converters.

Board monitoring

Board monitoring consists of unit temperature sensors and power information provided by the two PMICs. Power consuming components like the RF front end and DSP Unit are monitored in order to ensure operation within their specified envelope.

3.2.2 Software

The SatNOGS COMMS project requires the development of several software packages. All of the software will be released as open source under open source licenses. Due to the nature of the project, our goal is to use efficient, modern and open technologies, giving less effort to legacy systems.

DSP Software

The SatNOGS COMMS relies heavily on DSP software on both the ground and space segment. Each ground station is equipped with an SDR front-end. The front-end processes only digital I/Q samples. The rest of the required operations are implemented through DSP software. The SatNOGS ground stations utilize the gr-satnogs [4] software package, which is a GNU Radio [5] based module. This module is responsible for the filtering, re-sampling, demodulation and decoding of satellite signals. It is actively used on the SatNOGS network on more than 300 ground stations with transmission capabilities already under development.

The SatNOGS COMMS transceiver can operate in two different modes. The first one uses the hardware modem of the AT86RF215. In this mode, most of the DSP operations are implemented by the hardware modem of the IC. Only minor operations, like scrambling, interleaving are performed by the MCU. When the transceiver operates in I/Q mode, the majority of the DSP operations are executed by the FPGA IP cores. Figure 3.4 depicts the necessary functional blocks for the I/Q operational mode. On top of that, the ZYNQ-7020 IC provides also a dual core general purpose ARM processor. These cores are used to execute non time-critical DSP software re-used from gr-satnogs, like framing, CRC checks, etc.

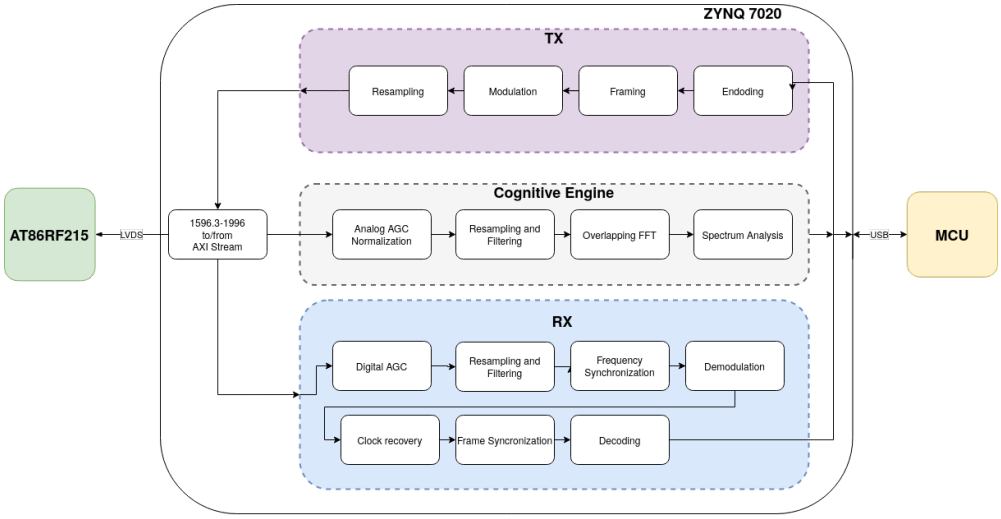

Figure 3.4: FPGA Block Diagram

FPGA IP Cores

The FPGA software is designed and implemented using the VPL paradigm. In this programming model, processing tasks are separated into functional blocks (named also IP Cores) and each block is completely independent from each other. Users can create programs by visually connecting the available blocks properly. This is a feature that is supported by the Vivado [6] design suite and widely used across several FPGA projects.

When applicable, the IP cores of the SatNOGS COMMS transceiver are implemented using the AXI4 [7] interconnect. AXI4 provides three different sub-types of interconnects AXI4, AXI4-Lite and AXI-Stream, each one suitable for different applications. For the DSP operations applied in the SatNOGS COMMS board, the AXI-Stream is used to pass information between the processing blocks. For asynchronous information exchange, (e.g. change filter parameters on the fly, change sampling rate, etc), the AXI4-Lite interconnect is used. Figure 3.5 is a use case of these interconnects. This specific IP core converts IQ samples from the IEEE 1596.3-1996 compliant LVDS interface of the AT86RF215 to two AXI4-Stream ports, one for the In-phase (port $M00\_AXIS\_I$) and one for the Quadrature (port $M00\_AXIS\_Q$) signal components. At the same time, the AXI4-Lite interconnect allows the user to dynamically change the functionality of the core asynchronously using the corresponding port (*port* $S00\_AXI\_CFG$). In this particular example, users can change the sampling rate on the fly using this configuration interface.

The choice of AXI4-Stream and AXI4-Lite interconnects was made to maximize reusability of existing DSP IP cores from Xilinx and have a standard and proven way of data exchange, while keeping the communication overhead as low as possible. The AXI4-Stream is ideal for point to point and stream oriented applications, which best matches the DSP operations that the board performs. On the other hand, the full AXI4 interconnect would be an overkill for simple data exchange, occupying vital resources. The use of AXI4-Lite deals with this issue and minimizes the resources utilization.

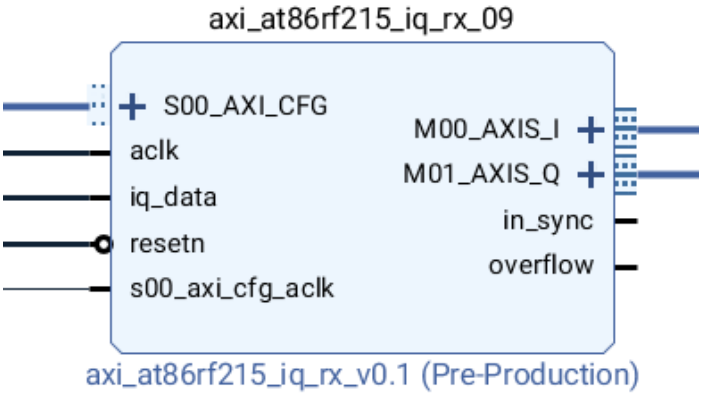

Figure 3.5: AT86RF215 LVDS IEEE 1596.3-1996 to AXI4-Stream IP core

Figure 3.4 presents in abstract way the basic principle of the DSP operations that the FPGA performs. However, each of the DSP tasks maybe implemented using one or more IP cores. These IP cores maybe provided by Xilinx, LSF or other vendors. We have taken measures so users can build the FPGA design without the need of a special Xilinx licence. So even if some IP cores are available from Xilinx (e.g. Viterbi decoder), it is not used it in the design. However, another implementation either from LSF or a third party vendor is used. In any case, LSF and third party IP cores are open source and can be synthesized without any special Vivado licence. Table 3.1 summarizes the IP cores used in the FPGA design along with the implementation vendor.

Controller Firmware

The firmware of the controller is responsible for interfacing with the board subsystems, gathering telemetry data, analyzing them and take the necessary actions for the well-being of the SatNOGS COMMS transceiver.

The MCU hosts the FreeRTOS [8] operating system, configured with static memory usage for all the internal functionality (queues, semaphores, stacks, etc). Actions will be made in order to ensure that no dynamic memory is used throughout the entire controller firmware. For accessing all the available peripherals of the MCU, the firmware makes use of the open-source HAL from STMicroelectronics [9]. The FreeRTOS tasks and queues operating in the MCU are shown in Figure 3.6.

IP cores	Vendors		
	LSF	**Xilinx**	**Others**
AT86RF215 IQ RX	✓		
AT86RF215 IQ TX	✓		
AXI4-Stream Math (+,-,*, etc)	✓	✓	✓
AXI4-Stream Complex multiplication		✓	
AXI4-Stream FFT		✓	
AXI4-Stream FIR filtering		✓	
AXI4-Stream CIC		✓	
CCSDS Scrambling	✓		
CCSDS Convolutional Coding	✓	✓	
CCSDS Viterbi Decoder	✓		
BPSK Modulator/Demodulator	✓		✓
FSK/MSK Modulator/Demodulator	✓		✓
Clock Recovery	✓		
Equalizer/Digital AGC	✓		
Frame construction	✓		
Frame synchronization	✓		
CRC Calculation	✓		✓
SPI Interconnect		✓	
USB Interconnect		✓	

Table 3.1: IP cores of the FPGA design and their vendors

Tasks.png

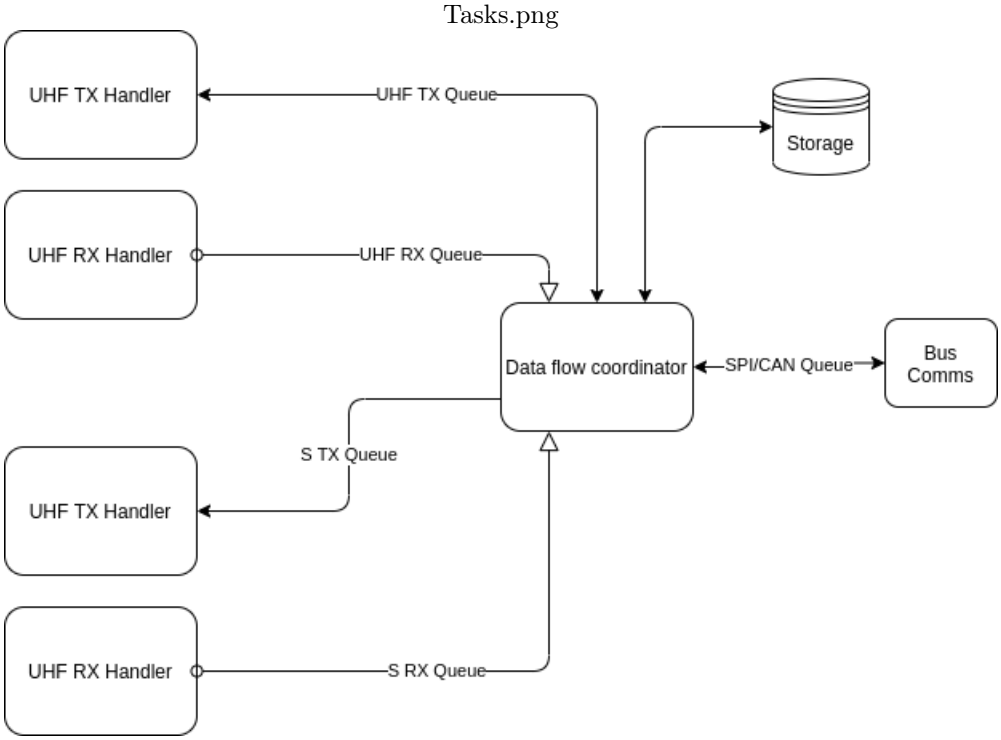

Figure 3.6: Tasks and Queues

IC Drivers

The SatNOGS COMMS transceiver accommodates several active ICs that need respective software to assist their functionality. The driver implementations for each IC are maintained on separate software repositories. Due to the diversity of the MCU execution environments and in order to maximize code re-usability, all of the drivers are implemented following a platform independent approach. Prior experience with this implementation scheme [10, 11] showed that this approach produces a more reliable, easy to test code-base that can be easily ported in other projects. Two drivers is expected to be developed; one for the AT86RF215 transceiver and one for the RFFC5071 RF mixer. To minimize dependencies and avoid concurrency issues (e.g.data or bus access races), each of the ICs is controlled exclusively by the MCU. Therefore, each of the drivers will be loaded and executed in the MCU. The available FPGA will act only as a DSP accelerator without any hardware direct access capabilities.

3.3 Design Rationale

Interface

An IO interface capable of out performing COMMS RF link capabilities while providing broad compatibility is implemented using a combination of CAN and SPI buses. For subsystems capable of CANFD, the CAN interface is sufficient for that scope. For subsystems supporting only CAN2.0, SPI is available for high speed data link while CAN2.0 is still used for control. This architecture allows for a Multi master SPI bus where several subsystems can communicate with COMMS. CAN is used for coordinating all SPI masters. CANFD protocol is compatible and can coexist with CAN 2.0 protocol.

Antenna Interface

Based on current market antenna solutions, antenna deployment is either handled by antenna its self via antenna controller with I2C interface or it is left to the user to implement the control part of the provided thermal knife or other deployment mechanism. For solutions having an antenna controller like GOMSpace NanoCom Ant-6f, Endurosat UHF Antenna III and ISISPACE CubeSat Antenna System for 1U/3U, I2C is exposed on the main connector. For solutions without a controller like NanoAvionics UHF Antenna System, COMMS provides activation and detection signal lines to be interfaced with the user's deployment controller. This approach is preferred since it provides great flexibility regarding the type of deployment controllers the user may choose to implement. These control lines are exposed on a dedicated connector and can also be exposed on the main connector.

Power supply

Digital parts are powered by a step down 3.3V DCDC converter which is monitored by external power monitor and supervisor. RF parts are powered by a step down 5V DCDC converter which is monitored by external power monitor and supervisor and additional LDO regulators for 3.3V RF parts. The variety of voltage levels needed by the FPGA unit requires multiple voltage regulators, load switches and power monitoring circuits. Due to the limited space available, PMICs provide an effective solution by integrating five voltage regulators in a single IC requiring minimal external components while providing full telemetry for all the outputs. PMICs are fully programmable and their startup operation depends on an OTP memory. Once startup sequence is completed, they can be reconfigured by the MCU. In the unlike event that this memory is corrupted by a SEU, PMIC may not be able to power up or output wrong voltage levels. For that reason memory contents are verified before startup and periodically from the MCU For an over-voltage misconfiguration to occur, both voltage output and over-voltage monitor registers must be corrupted in a way that will allow this to happen, this is considered a rare scenario, nonetheless, dedicated hardware voltage monitors are included to mitigate it.

Radio Transceiver

The majority of the COTS transceivers support only ISM band in [2400–2450] MHz and do not include the frequency bands defined by the requirements. During the initial design analysis several approaches were considered. One possible solution could be to use a full SDR approach using an IC that satisfies the frequency and bandwidth requirements. The candidate ICs that we investigated was the AD9364 [12] and the LMS7002M [13]. However, both of the ICs introduced two major drawbacks into the design. The first is related to the increased cost, due to the ICs cost itself and the more powerful FPGA that they require. The second one, which was also the reason that this approach was dropped, is related with the increased power consumption.

Another possible approach, would be to use IQ modulators and demodulators with integrated ADC and DAC. However, we could not find ICs to best fit the SatNOGS COMMS requirements. The majority of such ICs are wide band (»20 MHz bandwidth), resulting to a prohibitive power consumption starting from 3W.

Therefore, we decided to combine the benefits of a dedicated narrow-band transceiver and those of an SDR device, utilizing the AT86RF215 [1] IC. The bandwidth of the I/Q interface of this IC is only 4 MHz, reducing significantly the power consumption and the computational resources required. To meet the frequency requirements, a walking IF architecture is implemented only at the S-Band interface by using the RFFC5071 [14] as a RF mixer that produces the walking IF.

3.3.1 Fault detection, isolation, and recovery

SEU leading to FET/MOSFET latch

A MOSFET latch in the power segment can cause DCDC converter output to exceed design values leading to catastrophic failure of powered components. MOSFET latch recovery is carried out by power cycling affected DCDC converters and components via a hardware over voltage supervisor. PMIC although self supervised it can go into over voltage condition by memory misconfiguration/corruption. For such failure to occur both output and guard registers must fail in a way that allow over voltage conditions. As an added measure each PMIC output is monitored by hardware supervisors that power cycle the PMIC segment. A flowchart is provided in Figure 3.7

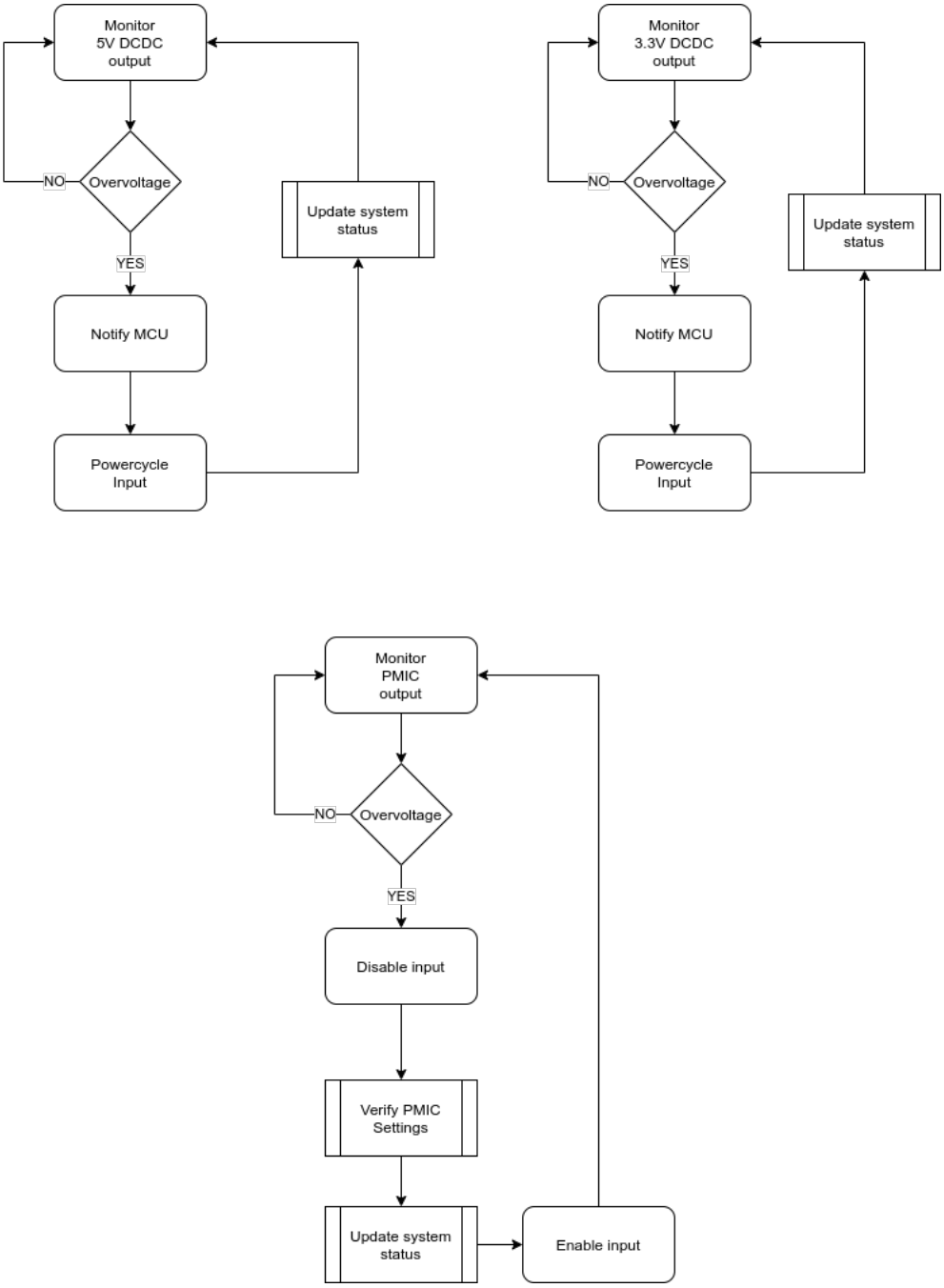

Figure 3.7: Power segment FDIR

RF component failure

RF components failure prevention and mitigation is shown in Figure 3.8

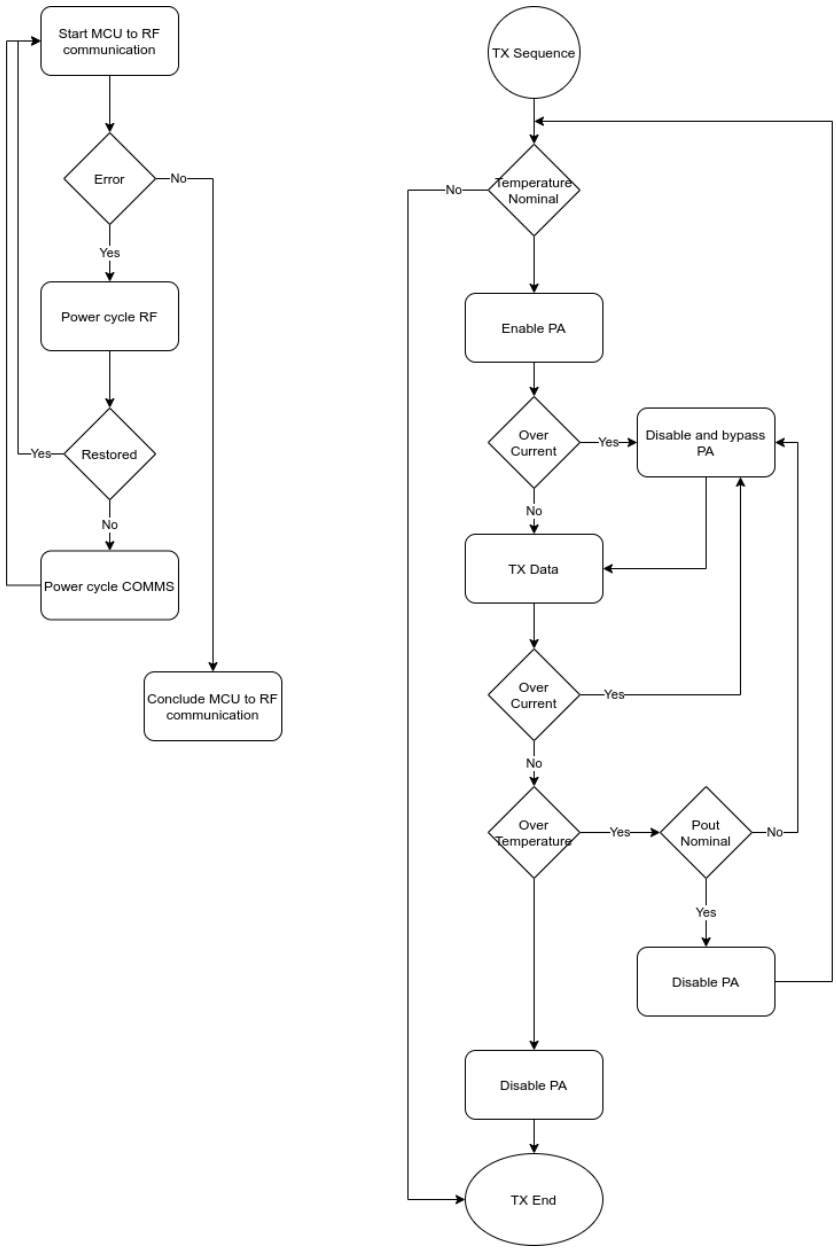

Figure 3.8: RF FDIR

UHF and S-Band segments can be independently isolated via load switches if a failure occurs allowing the remaining units to function properly. Load switches recovery from SEU is shown in Figure 3.9

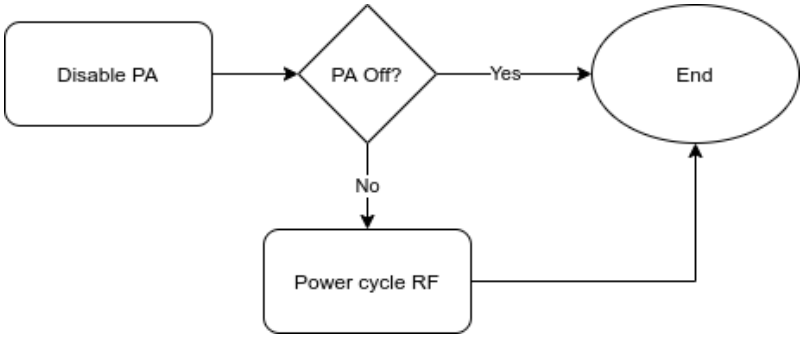

Figure 3.9: Load switch SEU recovery

Antenna disconnection/shorting

A shorted or disconnected antenna will increase power consumption and reduce PA power output as well as cause temperature increase. If such condition is detected, transmission will stop in order to protect RF components as shown in Figure 3.8

SEU leading to memory corruption

MCU memory ECC feature allows for detection of 2 errors and a single error correction. A memory scrubbing mechanism is implemented to reinstate recoverable data. If data correction is not possible, MCU will be reset. FPGA Memory has ECC implemented by the FPGA itself. Upon error detection, FPGA and its memory are reset.

SEU leading to firmware corruption

MCU memory ECC feature allows for detection of 2 errors and a single error correction. MCU boot-loader can verify flash contents by using a triple-stored CRC of memory contents. An identical backup firmware will be available to boot from. Defective firmware can be corrected based on valid firmware contents during flash memory scrubbing operation. Additional firmware copies can be stored in external storage if further redundancy is needed. Boot sequence is shown in Figure 3.10

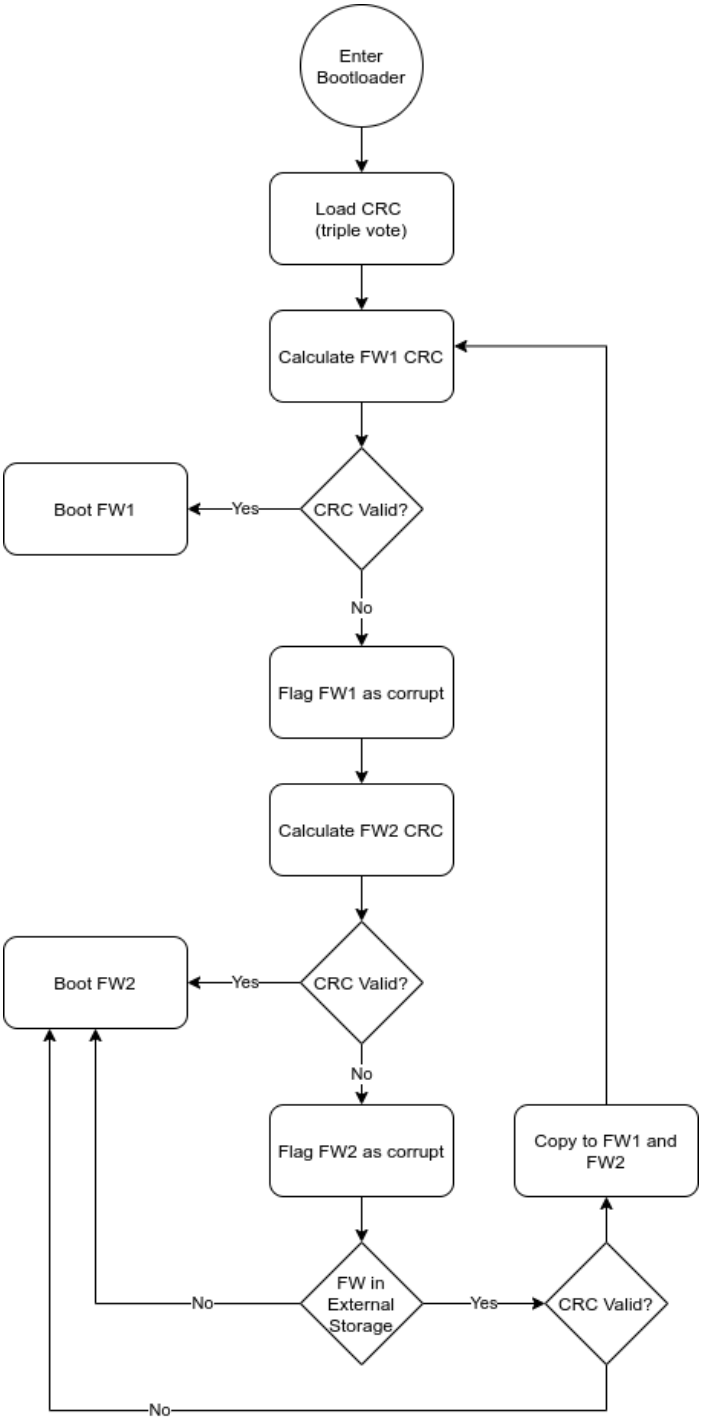

Figure 3.10: Boot sequence and firmware FDIR

4. Context

4.1 Actors

Satellite Operator

Satellite Operator, or Operator in the next 'Use Cases' session, is the person responsible for running communication, monitoring and housekeeping operations of a satellite mission.

Satellite Integrator

Satellite Integrator, or Integrator in the next 'Use Cases' session, is the person responsible for design and building the satellite.

4.2 Use Cases

Operator via SatNOGS Network communicates with satellite over UHF band

Operator, using a UI to connect with ground stations of SatNOGS Network, communicates with satellite over UHF band. Each communication is performed on configured UHF frequency with one of FSK, MSK or BPSK modulations, following a configured telecommunication schema and compensating expected Doppler shift.

Operator via SatNOGS Network communicates with satellite over S-band

Operator, using a UI to connect with ground stations of SatNOGS Network, communicates with satellite over S-band. Each communication is performed on configured S-band frequency with one of MSK, BPSK or QPSK modulations, following a configured telecommunication schema and compensating expected Doppler shift.

Operator via SatNOGS Network communicates with satellite over UHF and S-band

Operator, using a UI to connect with ground stations of SatNOGS Network, communicates with satellite over UHF and S-band at the same time. Each communication is performed on configured UHF or S-band frequency with one of FSK (only for UHF), MSK, BPSK or QPSK (only for S-band) modulations, following a configured telecommunication schema and compensating expected Doppler shift.

Operator monitors and analyses satellite telemetry data via configurable SatNOGS Dashboard

Operator, using a configured SatNOGS Dashboard to visualize telemetry data in form of time series, monitors and analyze satellite telemetry in almost real time.

Operator configures frequency and modulation of COMMS transceiver RX and TX

Operator is able to configure operating frequency and modulation of COMMS transceiver for receiving and transmitting independently for both UHF and S-band. For UHF, frequency is in 395–500 MHz frequency range and modulation is one of FSK, MSK or BPSK for both TX and RX. For S-band, frequency is in 2200–2290 MHz or 2400–2450 MHz frequency ranges for the TX and in 2025–2110 MHz, 2200–2290 MHz or 2400–2450 MHz frequency ranges for the RX and modulation is one of MSK, BPSK or QPSK for both TX and RX.

Operator configures frequency and modulation of ground station RX and TX

Operator is able to configure operating frequency and modulation of ground station for receiving and transmitting independently for both UHF and S-band. For UHF, frequency is in 395–500 MHz frequency range and modulation is one of FSK, MSK or BPSK for both TX and RX. For S-band, frequency is in 2200–2290 MHz or 2400–2450 MHz frequency ranges for the TX and in 2025–2110 MHz, 2200–2290 MHz or 2400–2450 MHz frequency ranges for the RX and modulation is one of MSK, BPSK or QPSK for both TX and RX.

Operator configures power of COMMS transceiver transmission

Operator is able to configure transmission power of COMMS transceiver to at least 30dBm.

Operator deploys antenna over UHF band

Operator deploys satellite antenna by sending telecommands via SatNOGS Network over UHF band. Deployment is confirmed through telemetry.

Operator deploys antenna over S-band

Operator deploys satellite antenna by sending telecommands via SatNOGS Network over S-band. Deployment is confirmed through telemetry.

Operator shuts down COMMS transceiver UHF subsystem over UHF or S-band permanently

Operator shuts down COMMS transceiver subsystem responsible for UHF transmissions by sending telecommands via SatNOGS Network either over UHF or S-band.

Operator shuts down COMMS transceiver S-band subsystem over UHF or S-band permanently

Operator shuts down COMMS transceiver subsystem responsible for S-band transmissions by sending telecommands via SatNOGS Network either over UHF or S-band.

Integrator configures initial UHF frequency and modulation of COMMS transceiver

Integrator sets the initial operating frequency and modulation of COMMS transceiver for receiving and transmitting independently for UHF band. Frequency is in 395–500 MHz frequency range and modulation is one of FSK, MSK or BPSK for both TX and RX.

Integrator configures initial S-band frequency and modulation of COMMS transceiver

Integrator sets the initial operating frequency and modulation of COMMS transceiver for receiving and transmitting independently for S-band. Frequency is in 2200–2290 MHz or 2400–2450 MHz frequency ranges for the TX and in 2025–2110 MHz, 2200–2290 MHz or 2400–2450 MHz frequency ranges for the RX and modulation is one of MSK, BPSK or QPSK for both TX and RX.

Integrator interconnects COMMS transceiver with other satellite subsystems

Integrator interconnects COMMS transceiver with other satellite subsystems. The interconnection with the subsystems is achieved through the interface connector, the antenna deployment electrical interface and the power supply electrical interface. Needed communication is achieved through CAN Bus protocol and/or SPI.

Integrator integrates physically COMMS transceiver with Satellite

Integrator integrates physically COMMS transceiver with Satellite via its mechanical interface and its calculated mass.

Integrator configures antenna deployment signal timing and signal type

Integrator configures signal timing and signal type for antenna deployment through the antenna deployment electrical interface.

Integrator configures antenna deployment handling from COMMS

Integrator configures antenna deployment to be handled by COMMS Software.

Integrator configures antenna deployment handling from subsystem

Integrator configures antenna deployment to be handled by another subsystem like OBC. COMMS responds on antenna deploy command and performs deployment.

5. Composition

5.1 Components

5.1.1 Hardware

Latest hardware design can be found at project's hardware repository[15]. Content is created and accessible using KiCAD[16] v5.1 and later. Latest hardware simulation designs can be found at project's hardware repository[15]. Content is created and accessible using Qucs[17] v0.0.2.

Digital Signal Processing Unit

For the required DSP operations the SatNOGS transceiver uses a ZYNQ-7020 FPGA. The speed grade of the transceivers of this particular FPGA family are more than enough to handle the LVDS interface of the AT86RF215 IC. In addition, this model have a set of DSP slices that is used for the implementation of the digital filters and the re-sampling required, significantly reducing the usage of other vital FPGA resources. An extra feature of this FPGA family, is the Dual-Core ARM Cortex-A9 processor that is available on the same die. These cores have a maximum frequency of 866 MHz and will be used for the less computationally intensive DSP tasks. The communication between the FPGA and the ARM processors is performed via an AXI4 [7] bus, minimizing the overhead and the latency. When idle, each of the two cores can be powered off to reduce the power consumption footprint.

Radio Transceiver

Our primary requirement is to select a transceiver that supports:

- Reading and writing raw complex I/Q samples with sampling rate of 4 MSPS and resolution of at least 12bits.
- Frequency range that is used for space communication, like [395–500] in UHF and [2025–2110], [2200–2290], [2400–2450]MHz in S-Band.
- Low power consumption, like 600mW.

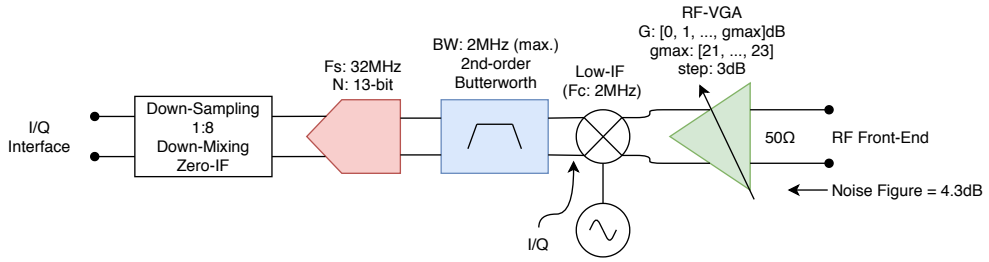

Figure 5.1: AT86RF215 Internal Receiver Architecture

The AT86RF215 [1] satisfies the requirement of I/Q interface, with 13-bit resolution and 4MSPS. The implemented interface is based on the IEEE 1596.3–1996 [18] standard. It also defines the maximum symbol rate of modulation schemes by the analog band pass filter (2nd-order Butterworth) in front of ADC with maximum bandwidth of 2MHz. The AT86RF215 [1] receiver follows a Low-IF architecture, with the IF at $Fc = 2MHz$. The RF front-end has an internal low noise, variable gain amplifier which is controlled either by an internal AGC or external by setting the registers of AT86RF215. This AGC is enabled in order to amplify the signal and to utilize the full resolution of ADC minimizing the quantization noise contribution. The internal AGC can be programmed to reduce the gain when an external LNA is present and compensate RSSI and EDV output values. Nevertheless, this mechanism supports only LNAs with fixed gains of 9 or 12dB so the performance of the AGC needs to be tested in conditions of weak signals and an external gain which is higher than 12dB. After the ADC a down-mixing to zero-IF and a down-sampling to 4MHz with anti-aliasing filters are implemented. The absolute maximum RX input level of AT86RF215 [1] is +10dBm while the maximum RX input level that fulfills the packet error rate of 10% is -5dBm. In our analysis for SQNR and ENOB of ADC, it was assumed that the full scale signal of ADC is -5dBm.

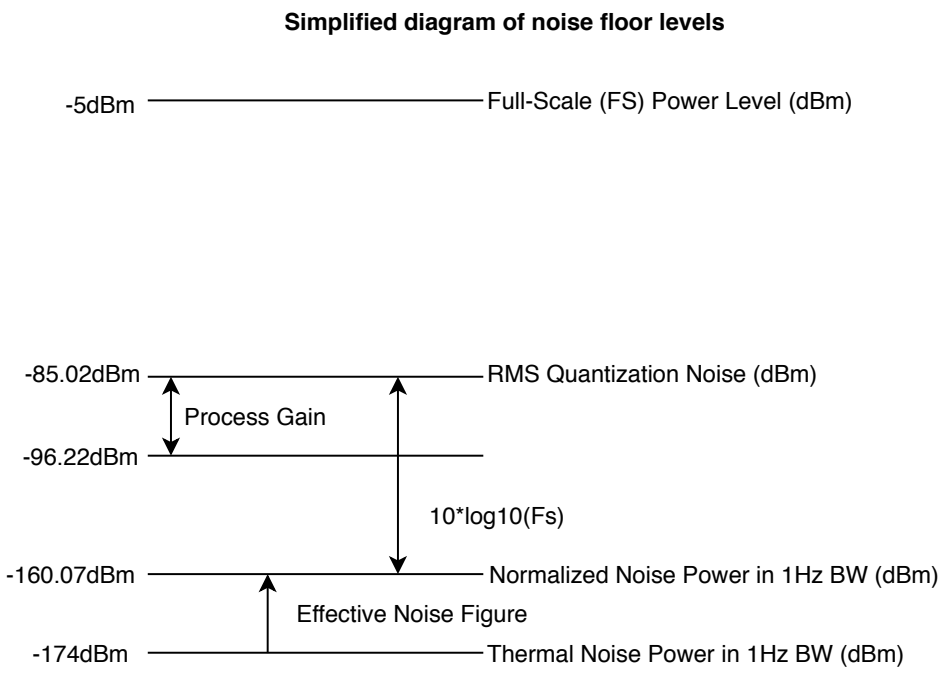

Figure 5.2: Simplified diagram of noise floor levels of ADC

As shown in figure 5.2 the noise power of converter is calculated by quantization noise $SQNR = 6.02 * b + 1.76$ of 13-bit (b) ADC and the process gain $\frac{Fs}{ENBW}$, with sampling rate $Fs = 32MHz$ and equivalent noise bandwidth for maximum bandwidth of 2nd order band pass filter in AT86RF215, $ENBW = 2.44MHz$, as calculated in Maxim AN:1929 [19]. For quantization noise the following assumptions are used:

- Theoretical quantization noise appears as white noise spread uniformly over Nyquist bandwidth, but in reality quantization noise appears concentrated at various harmonics.
- This noise depends of the ratio of the sampling frequency over the input signal.
- Input signal is a full scale sine wave.

The same input pins of AT86RF215 [1] are used for TX with 50Ω impedance. The TX architecture follows the zero-IF architecture, while the specifications of the DAC are the same with the ADC. After the DAC there is a programmable 2nd-order low pass filter with maximum cut-off frequency of 1MHz. The output level of AT86RF215 [1] is -10dBm to +14dBm with 1dB step.

The AT86RF215 transceiver has two balanced (50Ω) RF ports, one for sub-GHz and one GHz for UHF and S-Band respectively. The I/Q interface can not work simultaneously for both bands, due to common LVDS TX I/Q channel. Nevertheless,

the I/Q interface could operate simultaneously with the base band core which implements a sub-set of IEEE 802.15.4. Due to the requirement of half duplex in each band RF-switches are used. In case of S-Band a balun 50:50 and an unbalanced RF-switch is used. In case of UHF a balanced RF-switch is used. In both bands the switch must have:

- Low losses like 0.5dB.
- 1dB saturation point at least 20dBm, in order to handle the output power of AT86RF215 which is +14dBm.
- Isolation at least 20dB. The maximum output power of transmitter is +14dBm and the absolute maximum input RF level is +10dBm. An isolation between RF-switch ports of 20dB, means that when the AT86RF215 transmits +14dBm the receiver has a signal of +6dBm which is less than the absolute maximum input RF level.
- 50Ω impedance either balanced or unbalanced.
- Power supply and logic voltage compatible with 3.3V.
- Optionally, operation frequency range could cover both bands, DC-3000MHz.

Available options for RF switch and balun in S-Band are F2972 [20] and Johanson Technology 1720BL15B0050 [21] as shown in figure 5.3. Another selection for UHF band is the balanced RF-switch SKY13421–486LF [22]. The control logic of both RF-switch (for 2 bands) in input and output are done by RF front end control digital outputs of AT86RF215 in configuration 2 as described in data sheet (register RFn-PADFE).

RF Mixer

In S-band, the bands of interest are not satisfied by the tuning capabilities of the AT86RF215 [1], therefore an RF-mixer with integrated LO is used as shown in figure 5.3. The load switch of RF-mixer and RF-mixer are controlled by MCU as shown in figure 5.3.

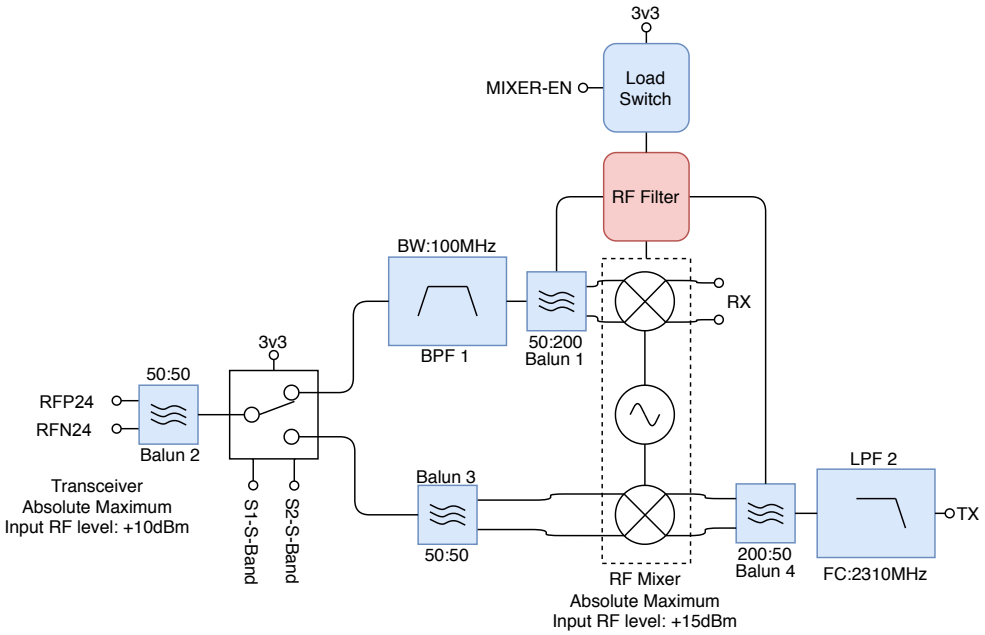

Figure 5.3: RF mixer and switch in S-Band

The LO frequency of the mixer must be between 80MHz to 4700MHz to down-convert or up-convert to the IF frequency of the AT86RF215 which is 2400MHz to 2483.5MHz. The RFFC5071 RF-mixer integrates in the same package two mixers, one for RX and the other one for TX. The output of both mixers is 200Ω differential (balanced). The input impedance depends on the mixer current setting which controls the input P1dB. The default mixer bias current register is set to 4 which is set the IP1dB to +12dBm to prevent saturation from AT86RF215 signal in TX mode. In RX mode, the mixer current register is set to 1 with IP1dB at +1dBm. Typical input impedance for these bias setting are 85Ω and 135Ω respectively. For that reason, a 50:50 balun (balun 3) like Johanson Technology 1720BL15B0050 [21] is used in TX path. In the input of RF mixer in both TX and RX, we have losses of 0.3dB and 1.03dB due to mismatch. For output impedance matching circuits are used a 4:1 impedance ratio, like Johanson Technology 1720BL15B0200 [23] (balun 1, 4). After the impedance matching of RX a band pass filter (BPF 1), like TDK DEA142450BT-3028A1 [24] or Qorvo 885071 [25] with a bandwidth of 100MHz, $Fc = 2450MHz$, insertion losses less than 3dB and impedance of 50Ω could be used to cut off any mixer artifacts like LO harmonics and image frequency. A look-up table 5.1 is used for optimal tuning of IF and LO to avoid mixing artifacts due to LO harmonics and to keep out the image frequency. Table 5.1 presents the values of image frequency, the IF, the LO, RF and the LO harmonics 5th, 6th, 7th.

Image (MHz)	IF (MHz)	LO (MHz)	RF (MHz)	5th LO (MHz)	6 LO (MHz)	7 LO (MHz)
1635	2415	390	2025	1950	2340	2730
1640	2420	390	2030	1950	2340	2730
1650	2430	390	2040	1950	2340	2730
1660	2440	390	2050	1950	2340	2730
1670	2450	390	2060	1950	2340	2730
1706	2434	364	2070	1820	2184	2548
1716	2444	364	2080	1820	2184	2548
1726	2454	364	2090	1820	2184	2548
1736	2464	364	2100	1820	2184	2548
1746	2474	364	2110	1820	2184	2548

Table 5.1: Look-up Table of LO frequencies of Receiver

We choose a LO frequency as high as possible, in order to keep away the image frequency [1635–1746]MHz and the harmonics of the LO. Also we select the LO frequency to be an integer multiple of the reference clock 26MHz. As referred in Appendix D, RF-mixer evaluation, for LO 400MHz the 5th, 6th and 7th harmonic are -60dBm, -50dBm and -60dBm. The 6th and 7th LO harmonics are the mixing artifacts that are passed to the internal mixer of AT86RF215. After the internal RF-mixer of AT86RF215, a band-pass filter with frequency response that follows a 2nd order Butterworth it exists. This filter at 75MHz, which is the 6th LO harmonic in base band (low-IF), away from the center frequency of 2MHz, it has losses near 60dB. Also the ADC sampling rate is 32MHz, which means in this bandwidth of $\pm$32MHz does not exist any mixing artifact. Figure 5.4 presents the response of impedance matching 1720BL15B0200 [23] and band-pass filter TDK DEA142450BT-3028A1 [24] by using S-parameters simulation in Qucs [17].

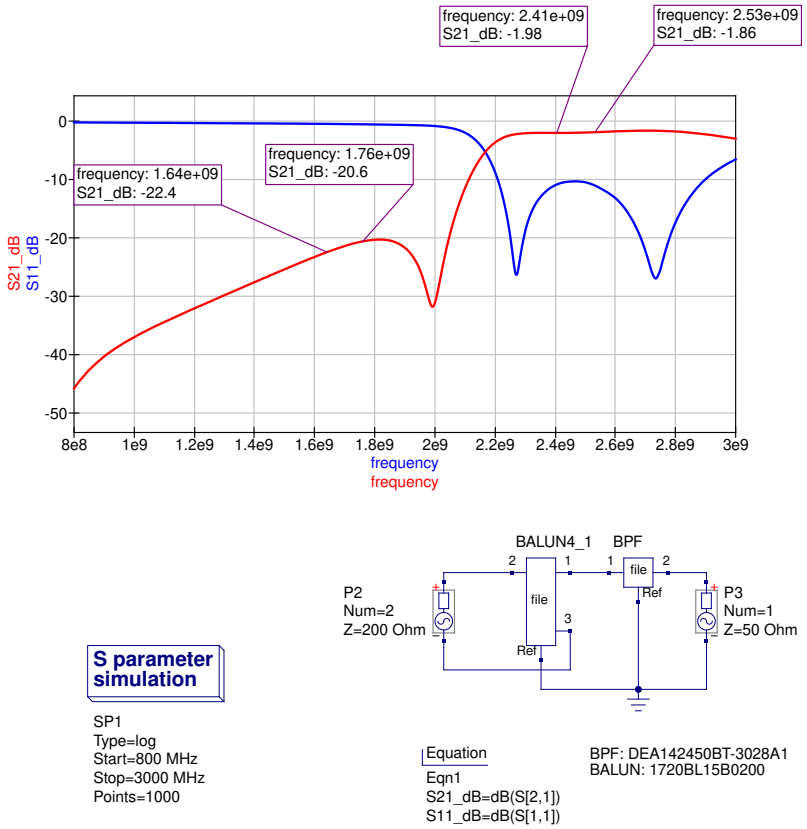

Figure 5.4: Impedance Matching and Image Rejection Filter Response

On the other hand the TX path must be compatible to SFCG 21–2R4 [26] recommendation 3 for low symbol rate spectral emission mask. According to FCC-ID VW4A092353 [27] the AT86RF215 [1] is compliant with the SFCG 21–2R4 [26]. In order the transmitter remains compatible with SFCG 21–2R4 [26] the LO harmonics and image frequency from RF mixer must be attenuated. The LO must be selected in order the image frequency to be as far as possible from the transmitting frequency. For that reason a look-up table 5.2 is developed.

Image (MHz)	IF (MHz)	LO (MHz)	RF (MHz)
7160	2480	4680	2200
7150	2470	4680	2210
7140	2460	4680	2220
7130	2450	4680	2230
7120	2440	4680	2240
7110	2430	4680	2250
7100	2420	4680	2260
7090	2410	4680	2270
7080	2400	4680	2280
7090	2400	4690	2290

Table 5.2: Look-up Table of LO frequencies of Transmitter

The low pass filter in figure 5.3, is designed to cut-off the minimum IF leakage with -10dB and other mixing products above the 2300MHz. The low pass filter is appeared in figure G.1 and is consist of low pass filter with passive elements (7th order Chebyshev). It is important to note that a worst case analysis for tolerances of sensitive passive components in low pass filter is done in appendix G. A test with RF-mixer evaluation board is done to evaluate the mixer output and the low pass filter response as shown in figure 5.6. In this stage the unwanted emission power level is approximately -45dBc measured in a reference bandwidth of 5kHz. The PA, as described in the next section 5.1.1, is working near to compression point 1dB and in combination with harmonic suppression filter in the output is achieved the maximum spurious level of -60dBc.

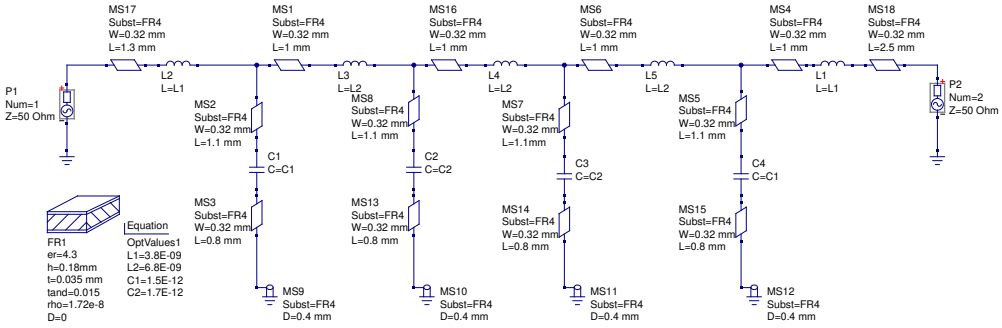

Figure 5.5: S-Band Low Pass Filter

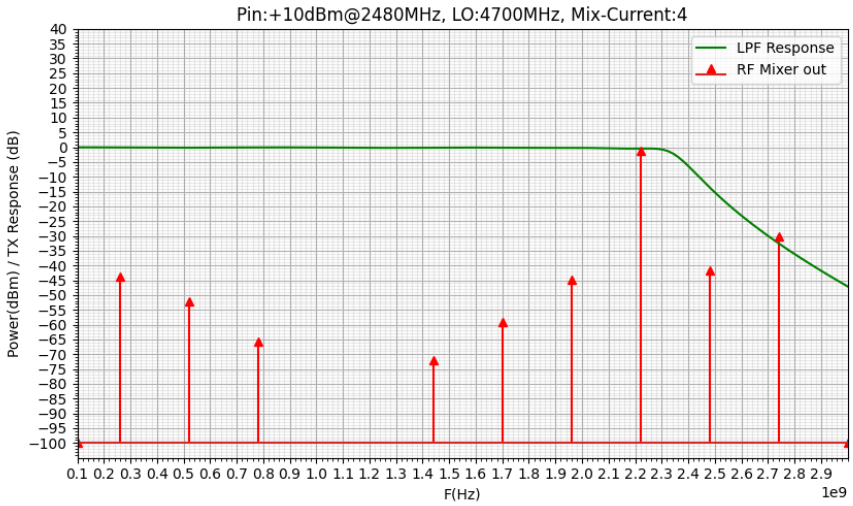

Figure 5.6: S-Band Low Pass Filter Response and RF Mixer Output

It is important to mention that the reference clock of RF-mixer must be the same with AT86RF215 [1] in order to avoid different drifts due to changes in operating conditions of reference clock. According to requirements the reference clock stability must be better than 20ppm. Both IC are needed a reference clock with typical 0.8Vp-p clipped sine wave of 26MHz. AT86RF215 [1] provides an output clock signal in pin 20 that would be used by the RF-mixer. The output clock signal driver strength is regulated by register (RF-CLKO) of AT86RF215 [1] which is set to 2mA. Also the crystal oscillator must be stable in environmental changes. An option would be the Kyocera Electronic Component TCXO, KT1612A26000AAW19TBT [28] with frequency stability 0.5ppm.

S-Band RF Front End

It is necessary to define the ground station transmitting EIRP and receiving signal, LEO losses and the satellite antenna, in order to define a range of receiving power in satellite antenna. Then according to this range the minimum and maximum gain of receiver is defined in order to minimize the noise figure while operating away from the P1dB saturation point. It is important to consider about the total power consumption of receiver. A same process is followed for TX, with more attention to the quality of the transmitting signal.

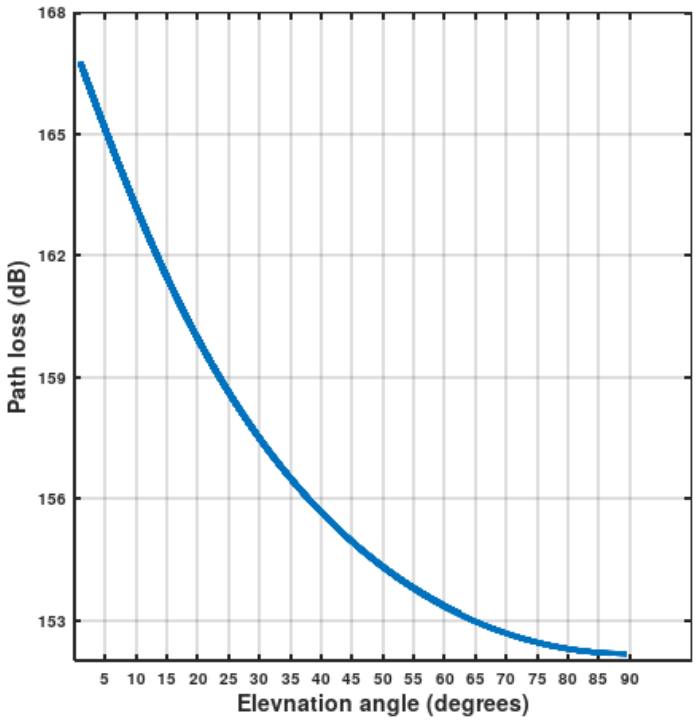

Figure 5.7: S-Band Path Loss

In this analysis the LEO losses is changed according to elevation angle and for a specific orbit, a constant EIRP is chosen. According to ECSS-E-ST-50-05C [29] the minimum elevation angle is 5 degrees and does not exist any restriction of maximum EIRP. For LEO losses calculations the gr-leo [30] software is used. This tool calculates the path loss taking into account atmospheric phenomena too, following the ITU-R P.619–3, P.676–11, P.618–13 and P.837–7 recommendations. Figure 5.7 presents a typical path loss scenario, at 2.3 GHz using the orbit of the ISS. For this particular example, the path loss at 5° of elevation is 167 dB, whereas at the apogee is around 152 dB.

The antenna system of a typical S-Band ground station for a satellite in 300–700km orbit is:

- A dish antenna with typical gain of 32dBi and beam width 5°.
- A power amplifier with typical transmitting power of 40dBm.

Some commercial ground stations justifying the above numbers are:

- Satlab Full-duplex S-band Ground Station

- GOMSpace S-Band ground station
- ISISpace S-band ground station

For this analysis we assume an EIRP of 71dBm as referred in table C.2. On the satellite, we consider an S-Band patch antenna with typical gain of 7dBi and beam width of ±40°. Some commercial S-Band patch antennas with such characteristics are the:

- EnduroSat S-Band Patch commercial Antenna
- GOMSpace NanoCom ANT2000
- IQ-Wireless S-Band Patch Antenna

Taking these characteristics into account, the signal level as received by the satellite should be between -93.3dBm to -77.3dBm. The main requirement for successful communication, is for the received Eb/N0 to be above the required Eb/N0 for each proposed modulation as shown in table C.2. According to ECSS-E-HB-50A [31] a BER of 10^{-5} should be considered for uplink budget calculations of Category A spacecrafts. In Appendix C are presented the link-budget tables. Fortunately, all of the CCSDS modulation and coding schemes that will be supported by the SatNOGS COMMS provide reliable communication with a margin of at least 3dB.

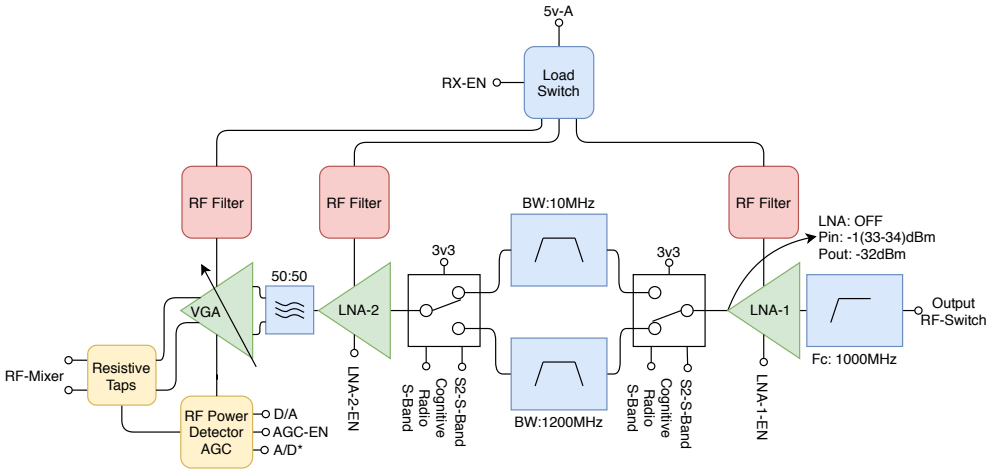

Figure 5.8: S-Band Receiver

The receiver in figure 5.8 contains a high pass filter (Fc:1000MHz) which cut off the UHF band in order to reduce the interference, due to concurrent operation of both radios. Figure 5.9 presents the response of HFCN-1000+ [32] high pass filter.

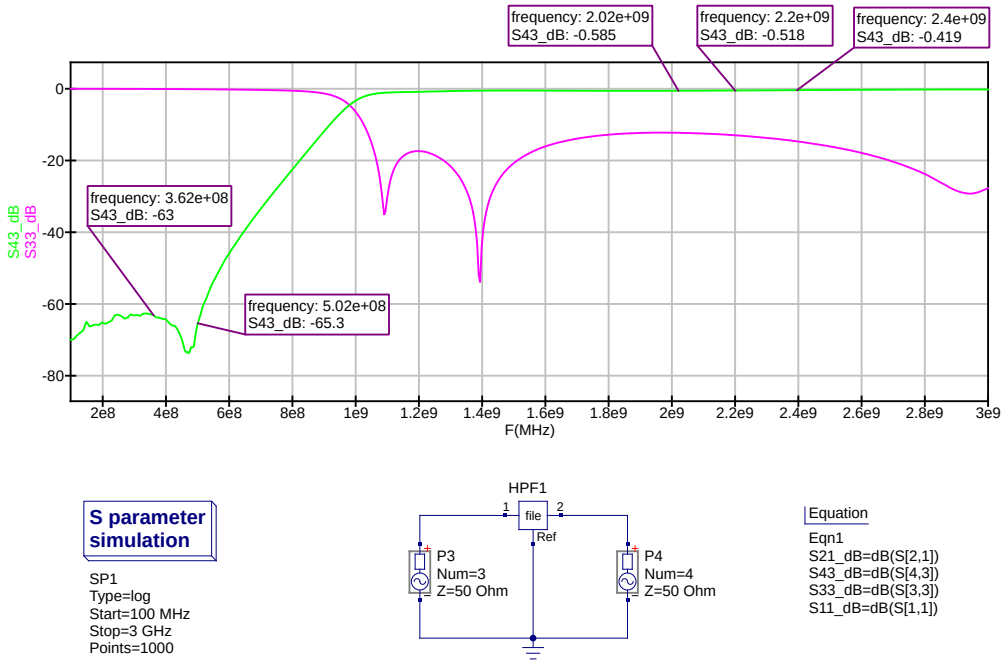

Figure 5.9: S-Band Notch Filter

Then, a wide band LNA-1 that increases the signal level and improves the overall noise figure of receiver. This LNA is critical to have noise figure less than 0.5dB and as possible as high gain. An option of COTS IC is QPL9057 [33] with NF less than 0.5dB and gain 22dB at 2200MHz.

It follows the cognitive radio implementation. It consists of two band pass filters:

- A narrow bandwidth of 10MHz, which increases the selectivity and improves the SNR of receiver. In case of a strong signal near the receiving frequency, the very sharp edges within the pass band of the filter cuts off almost any artifacts that are produced due to saturation of LNA-1. Also, the losses of 4dB are not limiting the dynamic range of receiver.

- A wide bandwidth of 400MHz, which permits to the receiver to listen frequencies out of receiving frequency and enables spectrum monitoring capabilities.

The switching between two filters is done by RF-switch which is controlled by MCU. Because we want a reduce BOM the RF-switch is F2972 [20] which is the same with the input RF-switch in antenna side. The wide bandwidth band pass filter is the component Mini Circuits BFCN-2491+ [34] with center frequency 2570MHz, bandwidth ±1240MHz and insertion losses 1.2dB (typical). The narrow BPF is selected according to operating frequency of RX. The table 5.3 contains SAW filters which available in the market.

Component	Fc(MHz)	Bandwidth(MHz)	Max Losses(dB)
SAWTRON - STA10789A	2040	94	5
SAWTRON - STA0892A	2040	60	5
SAWTRON - STA0886A	2096.66	40	5
Golledge - TA0741A	2067.5	84	4
Golledge - TA0892A	2067.5	84	4
Golledge - TA1079A	2040	60	5
Golledge - TA0886A	2096.66	40	5

Table 5.3: SAW Filters Characteristics

Both filters improves the SNR because the antenna cannot be considered as an effective filter when targets to the earth and receiving noise from bands outside the spectrum of interest which LNA-1 amplifies due to wide band operation bandwidth [600–4200]MHz. Before the signal inserts to RF-mixer must be amplified to compensate the conversion gain -7.5dB to -10dB, Appendix D, of it. For that reason an additional LNA-2 is added to receiver. Again, to reduce the BOM, we use QPL9057 [33]. The additional 10dB of gain helps the receiver to achieve a full scale signal in ADC. The NF it is not critical in this stage of RF chain.

The last functional block prior to RF-mixer is an analog AGC. The AGC is composed by:

- VGA, the maximum and minimum gain is defined by the minimum and maximum LEO losses in order to not saturate the receiver and to achieve a full scale input to ADC. The noise figure of this part it is not critical. The VGA gain control is done via an analog voltage that is produced by detector/controller. The gain step of VGA must be finer than the gain step of AT86RF215 VGA, 3dB, for a more accurate tuning of AGC. The gain control span of VGA must be the same or near the dynamic range of detector/controller.

- Detector/Controller, the dynamic range of detector must be capable to detect signal in range of $[-50, -10]dBm$ with a error of $\pm 1dB$. The controller it gets a set point, analog voltage, that defines the power level in the output of VGA.

- Resistive tap, it used by detector/controller to get feedback of power level in the output of VGA. The coupling factor of tap is defined by the maximum RF input of detector. The resistive tap is ideal for this application due to low complexity and almost same response in a wide range of frequencies in case of spectrum monitoring capabilities.

To implement the AGC, we use a proposed solution from Analog Devices application note AN–1507 [35]. This approach covers a wide range of frequency $10 - 3000MHz$. The VGA is ADL5330 [36] and the detector/controller is AD8318 [37].

The ADL5330 [36] input and output are 50Ω balanced lines. For input it is used a balun with impedance ratio 1 : 1. A choice could be 1720BL15B0050 [21]. The output is connected to a resistive tap and to RF-mixer. As referred in Section 5.1.1 the input impedance of RF-mixer is 135Ω. This impedance mismatch from 50Ω to 135Ω introduces losses of 1.03dB. In order to calculate the resistive tap coupling factor it is necessary to calculate the cascade saturation point 1dB and the IP3 with maximum gain of VGA. In figure 5.12 is presented all the S-Band RF front-end and in the tables 5.4 - 5.7 all S-Band receiver components.

Component	SP2T	HPF	LNA-1
Gain (dB)	-0.4	-0.4	19
Noise Figure (dB)	0.4	0.4	0.5
IIP3(dBm)	77	2000	10
IP1dB (dBm)	40	2000	-4
Bandwidth (MHz)	5–10000	—	600–4200
Fc (MHz)	—	1000	—
DC-Power (mW)	0.495	—	250
Part Number	F2972	HFCN-1000+	QPL9057

Table 5.4: S-Band Receiver Components — Part 1, Characteristics

Component	SP2T	BPF	SP2T	LNA-2
Gain (dB)	-0.4	-3	-0.4	19
Noise Figure (dB)	0.4	3	0.4	0.5
IIP3 (dBm)	77	2000	77	10
IP1dB (dBm)	40	2000	40	-4
Bandwidth (MHz)	5–10000	84	5–10000	600–4200
Fc (MHz)	—	2067.5	—	—
DC-Power (mW)	0.495	0	0.495	250
Part Number	F2972	Golledge TA0892A	F2972	QPL9057

Table 5.5: S-Band Receiver Components — Part 2, Characteristics

Component	Balun	VGA	Resisitive Taps	Mismatch
Gain (dB)	-1.5	9	-1	-1.03
Noise Figure (dB)	1.5	12.5	1	1.03
IIP3 (dBm)	2000	5	2000	2000
IP1dB (dBm)	2000	-1.7	2000	2000
Bandwidth (MHz)	625–2815	10–3000	400	—
Fc (MHz)	—	—	2200	—
DC-Power (mW)	0	1075	0	0
Part Number	1720BL15B0050	ADL5330	In-House	—

Table 5.6: S-Band Receiver Components — Part 3, Characteristics

Component	Mixer	Balun	BPF	SP2T	Balun
Gain (dB)	-8.5	-1.5	-1	-0.4	-1.5
Noise Figure(dB)	12	1.5	1	0.4	1.5
IIP3 (dBm)	10	2000	2000	77	2000
IP1dB (dBm)	1	2000	2000	40	2000
Bandwidth (MHz)	85–2700	625–2815	100	5–10000	625–2815
Fc (MHz)	—	—	2450	—	—
DC Power(mW)	412.5	0	0	0.495	0
Part Number	RFFC 2051	1720BL15 B0200	DEA142450 BT–3028A1	F2972	1720BL15B0050

Table 5.7: S-Band Receiver Components — Part 4, Characteristics

A design choice is to select a power level in output of receiver -45dBm (adding P1dB Back-off of -15dB) which is below the IP1dB of AT86RF215 as shown in table 5.9. This value of operation is below of OP1dB of receiver as shown in table 5.8. The coupling factor of resistive tap is calculated in order this $OutputPowerLevel - RF - mixerGain - CouplingFactor$ must be inside the dynamic range ($\pm 3dB$) from -5dBm to -65dBm of AD8318. Also the coupling factor must be greater than -10dB due to limit in insertion loss of -2.5dB that will introduce in RF chain. A coupling factor of -10dB is selected. The input power level in the detector is -46.5dBm which fullfil

the requirement of measurement error of $\pm 1dB$. The power level output of receiver could be changed by MCU and the setting gain of VGA could be measure by MCU and FPGA.

Component	Receiver
Gain (dB)	33.97 (maximum)
NF(dB)	1.41
OP1dB (dBm)	-13.22
OIP3 (dBm)	-3.42

Table 5.8: S-Band Receiver cascade characteristics

Component	AT86RF215
Gain (dB)	23 (maximum)
NF(dB)	4.3
IP1dB (dBm)	-29.4
IIP3 (dBm)	-15

Table 5.9: S-Band AT86RF215 Receiver characteristics

The minimum input signal that the AGC operates is calculated -82dBm as shown in figure 5.10(maximum gain of VGA).

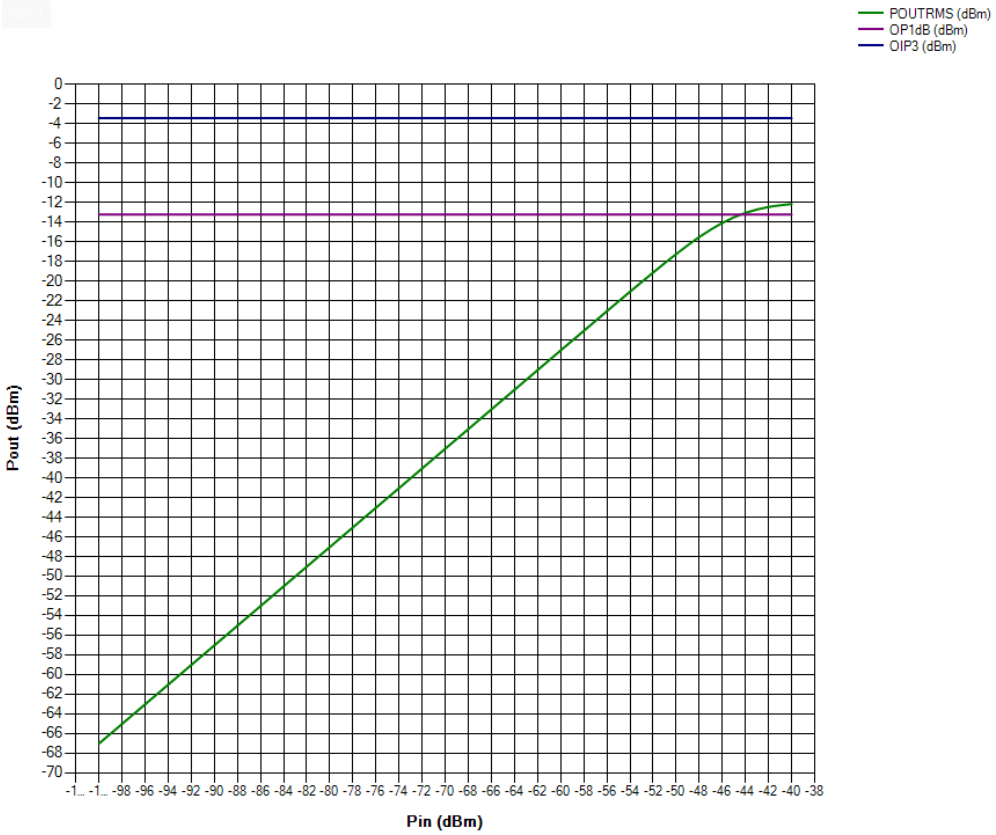

Figure 5.10: S-Band Front-End Output Power

In order to design the resistive tap with coupling factor of -10dB, we use the impedance $28 - j102\Omega$ of AD8318 [37] at 2200MHz. A Qucs simulation gives us the insertion loss (S21) and the coupling factor (S31) of the tap in figure 5.11. The P1 power source is the input of RF-mixer, P2 is the output of VGA and P3 is the detector input. The losses due to impedance mismatch are included. The selected resistor for tap is ERA-2AEB620X [38] with 1% tolerance and temperature coefficient $25PPM/C$.

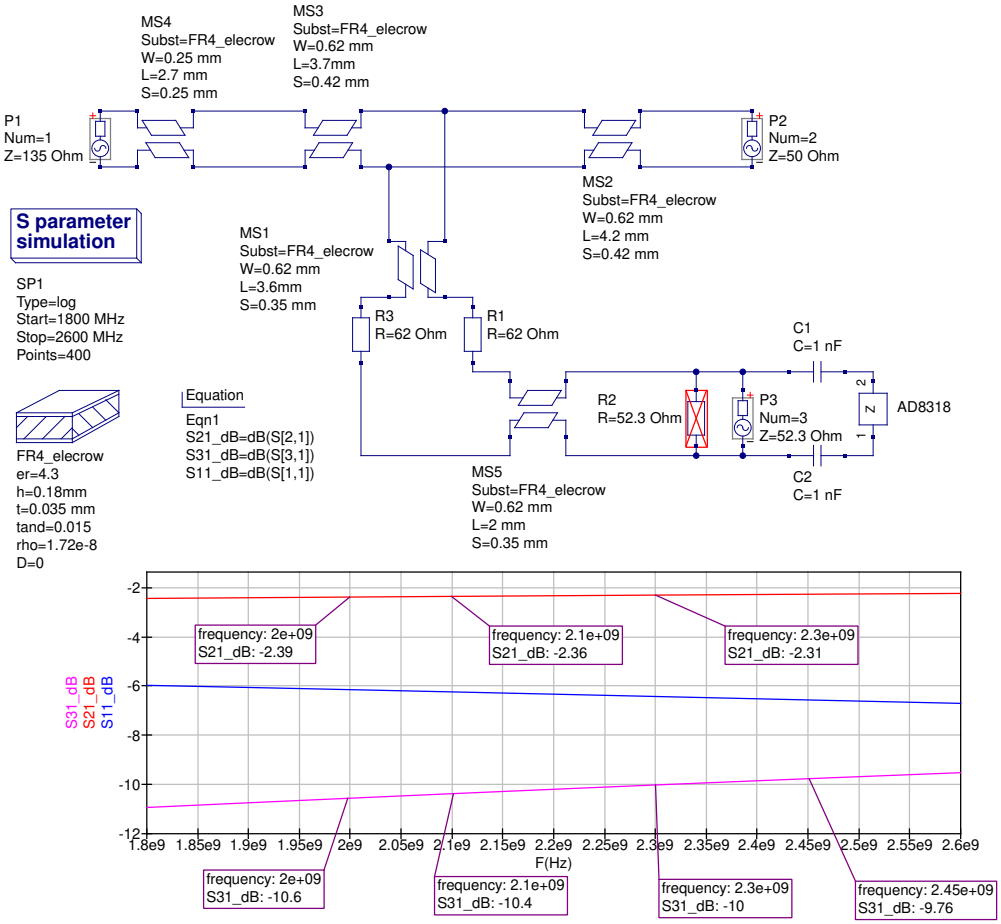

Figure 5.11: S-Band Resistive Tap Coupling factor (S31) and Insertion Loss (S21)

The AGC protects the receiver from a strong signal that it could destroy components of the receiver like the RF-mixer and transceiver which the absolute maximum RF input is +15dBm and +10dBm respectively. Another import thing is to protect the receiver when the transmitter in enabled. The isolation of the RF-switch before the antenna must be at least -35dB. When the front-end transit signal of +30dBm in the input of receiver the signal level is -5dBm which is smaller than the maximum RF input of QPL9057 [33] (+27dBm OFF mode). According to data-sheet of QPL9057 [33] the OFF mode gain when the input signal is -5dBm is -35dB, thus the output signal of LNA-1 is -40dBm. By using the AGC and the wide bandwidth BPF, while the transmitter is enabled, the detector AD8318 could measure the output power which is useful in failure detection as described in Section 3.3.1. An option for RF-switch before the antenna is F2972 [20], with typical isolation between common port and input ports is -37dB and low insertion losses of -0.4dB at 2000MHz to 3000MHz

bandwidth. The control logic of S-Band receiver is designed in order to enable/disable every stage separately. The main load switch in figure 5.8 is control all the RX stages. Each of amplifiers and AGC are controlled by MCU via pins, AGC-EN, LNA-2-EN and LNA-1-EN.

The radio, also supports transmission in S-Band. Before starting to analyze the transmitter front-end architecture is critical to calculate the link budget. As mention above the LEO losses are 152–167dB, the satellite antenna gain is 7dBi and the ground station antenna is 32dBi. Lets calculate the minimum and maximum signal in the ground station receiver. We assume the satellite transmitting power at least 30dBm, due to maximum available power of 8.3W and to low efficiency 35% (∼3.5W) of high linearity power amplifier. The minimum receiving signal is -102.1dBm and the maximum is -85.5dBm. As shown in table C.3, the margin in case of 5 degrees is above the limit of 3 dB that provides reliable communication.

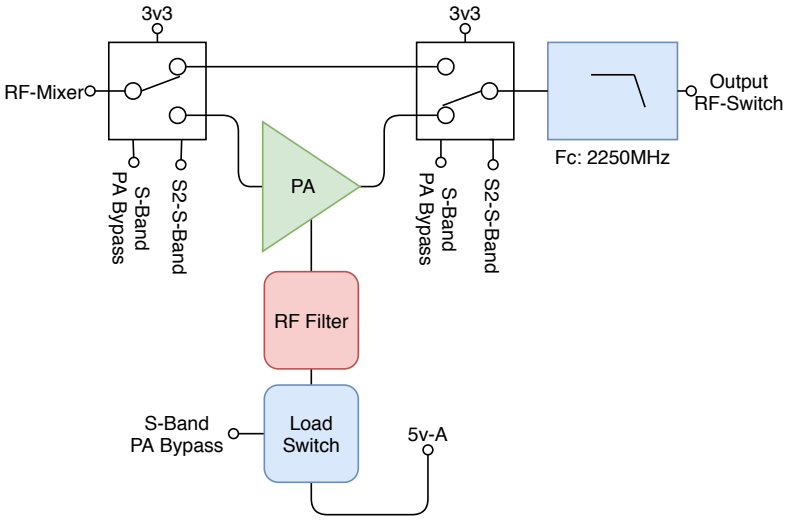

Figure 5.13: S-Band Transmitter Front-End

The transmitter is appeared in figure 5.13. After the RF mixer, the main amplifier and the recovery mechanism of it are followed. The RF-switches, as appeared in figure 5.13, are used to bypass the power amplifier when a failure is detected on it, as described in Section 3.3.1. An option for RF-switch is F2972 [20]. The same RF-switch is used before the antenna.

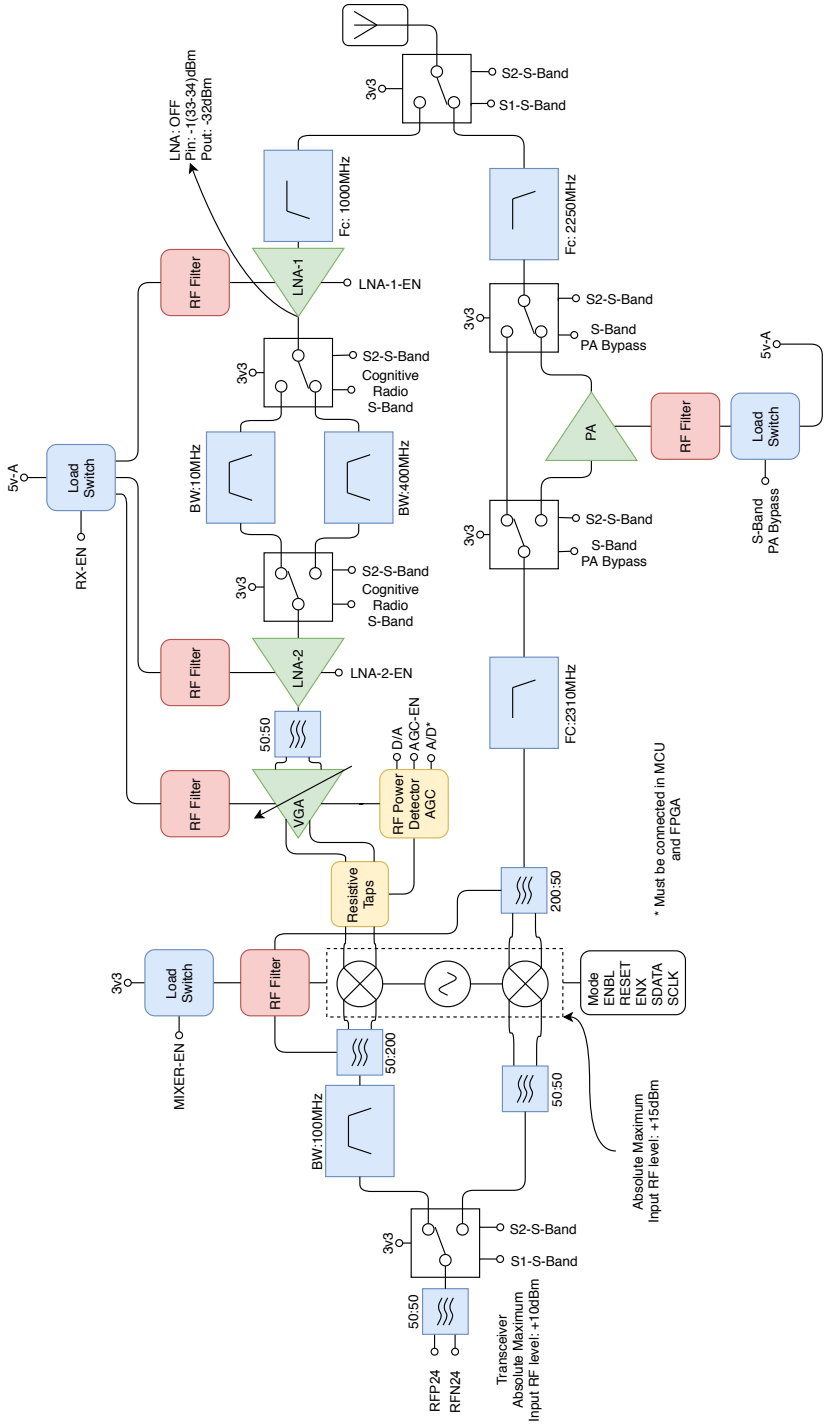

Figure 5.12: S-Band Front-End

Component	Balun	SPDT	Balun	Mismatch	Mixer	Balun
Gain (dB)	-1.5	-0.4	-1.5	-0.3	-8.5	-1.5
Noise Figure(dB)	1.5	0.4	1.5	0.3	12	1.5
OIP3(dBm)	2000	76.6	2000	2000	16.9	2000
OP1dB (dBm)	2000	38.6	2000	2000	2.5	2000
Bandwidth (MHz)	625-2815	5-10000	625-2815	—	85-6000	625-2815
DC Power(mW)	0	0.495	0	0	412.5	0
Part Number	1720BL 15B0050	F2972	1720BL 15B0050	—	RFFC 5071	1720BL 15B0200

Table 5.10: S-Band Transmitter Components — Part 1, Characteristics

The output power of AT86RF215 is selected to be between +5dBm to +12dBm. The maximum power level of AT86RF215 is selected to not saturate the RF-mixer, as referred in Appendix D. Before we define the gain of power amplifier, we must define the PAPR of supported modulations, table 5.11.

Modulation	PAPR (dB)
BPSK	3
QPSK	1.8
MSK	3.3

Table 5.11: PAPR of Supported Modulations

It is necessary to amplify the signal in order to achieve a power output of +30dBm at least with peaks at +33dBm due to modulations. The output power is controlled by the internal VGA of AT86RF215 [1] with +1dB step. The frequency range of power amplifier must be 2200MHz–2290MHz and 2400MHz–2450MHz. The gain of amplifier must be +34dB. An option of PA could be SKY66292–11 [39]. As described in section 5.1.1, it is needed to attenuate:

- -15dB the IF leakage (2400MHz - 2480MHz).
- Mixing artifacts like $3*IF-2*LO$ which are below 2200MHz could be attenuated by PA response

in order to be SFCG 21–2R4 [26] compliant. An additional low pass filter(Fc:2250MHz) is used as it is appeared in figure 5.13 with corner frequency near to the first 7th

order low pass filter (2310MHz). An option could be the LFCG-2250+ [40] with power handling of 5W. In the table 5.12 are presented the remaining components of transmitter.

Component	LPF	SPDT	PA	SPDT	LPF	SPDT
Gain (dB)	-1	-1	35	-0.4	-1.2	-0.4
Noise Figure (dB)	1	0.4	N/A	0.4	1.2	0.4
OIP3 (dBm)	2000	76.6	49.4	76.6	2000	76.6
OP1dB (dBm)	2000	38.6	35	38.6	2000	38.6
Bandwidth (MHz)	—	5–10000	2200–2290	5–10000	—	5–10000
Fc (MHz)	2310	—	—		2250	—
DC Power (mW)	0	0.495	3500	0.495	0	0.495
Part Number	In-house	F2972	SKY66292–11	F2972	LFCG-2250+	F2972

Table 5.12: S-Band Transmitter Components — Part 2, Characteristics

In the figure 5.14 and the table 5.13 are presented the cascade characteristics of transmitter.

Component	Transmitter
Gain (dB)	17.9
OP1dB (dBm)	28.6
OIP3 (dBm)	44.2

Table 5.13: S-Band Transmitter cascade characteristics

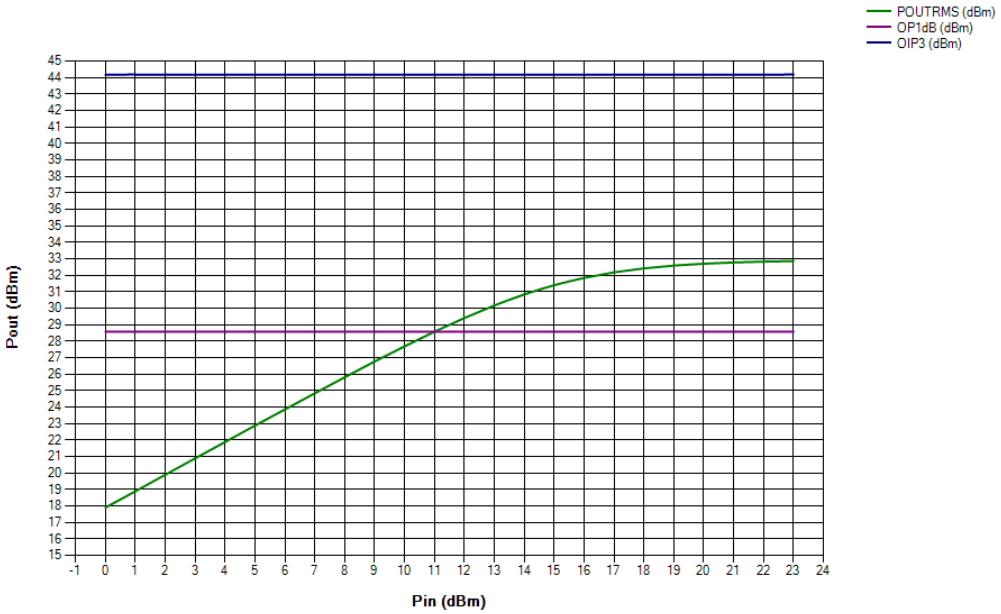

Figure 5.14: S-Band Transmitter Output Power

In figure 5.15 is shown the output of RF mixer and the response of TX chain. In this stage the unwanted emission power level is calculated approximately -58dBc.

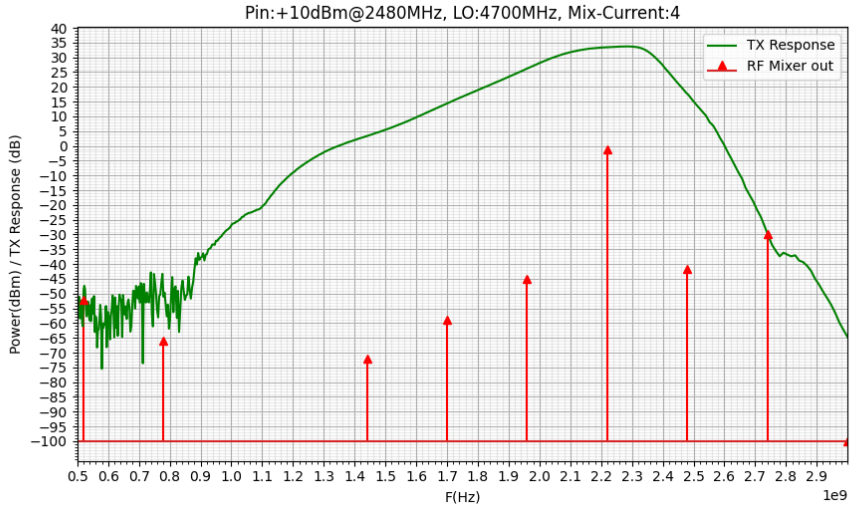

Figure 5.15: S-Band Transmitter Front-End, Qucs simulation

UHF RF Front End

As defined in S-Band radio with a same way, it is necessary to define the ground station transmitting EIRP, LEO losses and the satellite antenna, in order to define a range of receiving power in satellite antenna.

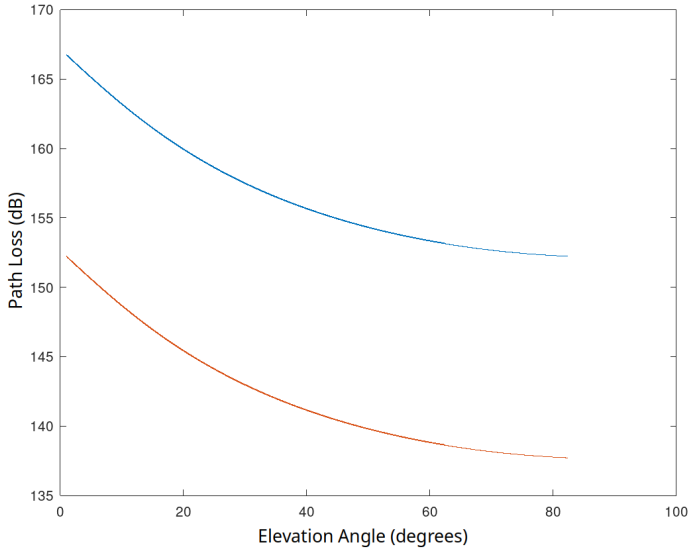

Figure 5.16: UHF (Red) and S-Band (Blue) Path Loss

Figure 5.16 presents a typical path loss scenario using frequency 430MHz, orbit of the ISS and same parameters as defined in S-Band path loss analysis. For this particular example, the path loss at 5° of elevation is 153dB, whereas at the apogee is around 137dB.

The antenna system of a typical UHF ground station for a satellite in 300–700km orbit is consist of a circular polarization antenna with typical gain of 16dBi and beam width 36° and a power amplifier with typical transmitting power of 47dBm. Some commercial ground stations justifying the above numbers are:

- GOMSpace NanoCom AS100 ground station
- ISISpace VHF/UHF Ground Station

For this analysis we assume an EIRP of 62dBm as shown in table C.4.

On the satellite, we consider a circular polarization, turnstile antenna with typical gain of 1.4dBi and radiation pattern close to omni-directional. Some commercial UHF antennas with such characteristics are the:

- EnduroSat UHF Antenna

- GOMSpace NanoCom ANT430
- ISISpace CubeSat Antenna System for 1U/3U
- NanoAvionics UHF Antenna System

Taking these characteristics into account, the signal level as received by the satellite should be between -91.8 to -74.8dBm. The main requirement for successful communication, is for the received Eb/N0 to be above the required Eb/N0 for each proposed modulation as shown in table C.4. According to ECSS-E-HB-50A [31] a BER of 10^{-5} should be considered for uplink budget calculations of Category A spacecrafts. In Appendix C are presented the link-budget tables. Fortunately, all of the CCSDS modulation and coding schemes that will be supported by the SatNOGS COMMS provide reliable communication with a margin of at least 3 dB as described in ECSS-E-ST-50-05C [29].

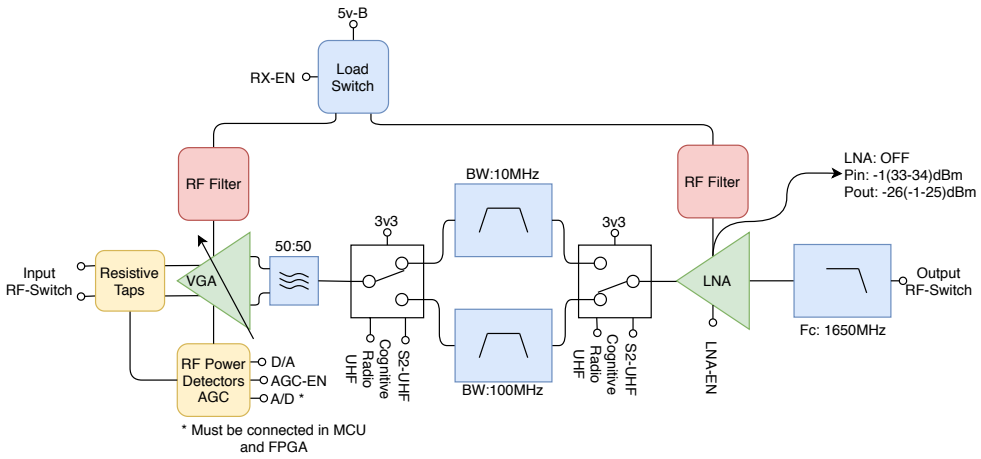

Figure 5.17: UHF Receiver

The receiver in figure 5.17 contains a low pass filter (Fc:1650MHz) which cut off the S-Band in order to reduce the interference with other radio. A possible component could be LFCG-1400+[41].

Then, a wide band LNA that increases the signal level and improves the overall noise figure of the receiver. An option could be TQP3M9036[42] with 24dB gain and 0.4dB noise figure at 450MHz.

As in S-Band receiver, a cognitive radio implementation it follows.

The narrow BPF is selected according to operating frequency of RX. The table 5.14 contains SAW filters which available in the market.

Component	Fc(MHz)	Bandwidth(MHz)	Max Losses(dB)
AFS403.5W01-TS3	403.5	4	4.5
SAWTRON - STA1135A	403.5	7.6	2.5
Golledge - TA0980A	402	4	4.5
Taoglas - DBP.433.T.A.30	433.92	10	3
SAWTRON - STA0693A	435	10	3.3
Golledge - TA0693A	435	10	3.3
Golledge - TA1408A	435	10	3.5
AFS434S3	434	4	4.5

Table 5.14: SAW Filters Characteristics

The wide band filter with bandwidth of 100MHz it could be the BFTC-500+[43]. The same RF switch as in S-Band is used, F2972[20].

The last functional block prior to transceiver is an analog AGC. The same VGA and detector-controller with S-Band is used. Because of the balanced lines of VGA a 1:1 balun is used, with part number ATB2012–50011-T000[44]. In order to calculate the resistive tap coupling factor it is necessary to calculate the cascade saturation point 1dB and the IP3 with maximum gain of VGA. In tables 5.15 — 5.18 are presented the components of receiver as shown in figure 5.20.

Component	SP2T	LPF	LNA
Gain (dB)	-0.4	-0.3	24
Noise Figure (dB)	0.4	0.3	0.4
IIP3(dBm)	77	2000	12
IP1dB (dBm)	40	2000	1
Bandwidth (MHz)	5–10000	—	5–2000
Fc (MHz)	—	1000	—
DC-Power (mW)	0.495	—	340
Part Number	F2972	LFCG-1400+	TQP3M9036

Table 5.15: UHF Receiver Components — Part 1, Characteristics

Component	SP2T	BPF	SP2T
Gain (dB)	-0.4	-4	-0.4
Noise Figure (dB)	0.4	4	0.4
IIP3 (dBm)	77	2000	77
IP1dB (dBm)	40	2000	40
Bandwidth (MHz)	5–10000	4	5–10000
Fc (MHz)	—	434	—
DC-Power (mW)	0.495	0	0.495
Part Number	F2972	AFS434S3	F2972

Table 5.16: UHF Receiver Components — Part 2, Characteristics

Component	Balun	VGA	Resisitive Taps
Gain (dB)	-1	22	-0.7
Noise Figure (dB)	1	7.2	0.7
IIP3 (dBm)	2000	13.9	2000
IP1dB (dBm)	2000	1.3	2000
Bandwidth (MHz)	40–860	10–3000	400–500
Fc (MHz)	—	—	450
DC-Power (mW)	0	1075	0
Part Number	ATB2012–50011–T000	ADL5330	In-House

Table 5.17: UHF Receiver Components — Part 3, Characteristics

Component	DPDT
Gain (dB)	-0.5
Noise Figure(dB)	0.5
IIP3 (dBm)	55
IP1dB (dBm)	24
Bandwidth (MHz)	100–3000
Fc (MHz)	—
DC Power(mW)	0.0495
Part Number	SKY13421–486LF

Table 5.18: UHF Receiver Components — Part 4, Characteristics

A design choice is to select a power level in output of receiver -42dBm (adding P1dB Back-off of -15dB) which is below the IP1dB of AT86RF215 as shown in table 5.20. This value of operation is below of OP1dB of receiver as shown in table 5.8. The coupling factor of resistive tap is calculated in order this $OutputPowerLevel - CouplingFactor$ must be inside the dynamic range ($\pm 3dB$) from -5dBm to -65dBm of AD8318. Also the coupling factor must be greater than -10dB due to limit in insertion loss of -1.5dB that will introduce in RF chain. A coupling factor of -12dB is selected. The input power level in the detector is -50dBm which fullfil the requirement of measurement error of $\pm 1dB$. The power level output of receiver could be changed by MCU and the setting gain of VGA could be measure by MCU and FPGA.

Component	Receiver
Gain (dB)	38.3 (maximum)
NF(dB)	1.38
OP1dB (dBm)	18.7
OIP3 (dBm)	34.58

Table 5.19: UHF Receiver cascade characteristics

Component	AT86RF215
Gain (dB)	23 (maximum)
NF(dB)	4.3
IP1dB (dBm)	-27.4
IIP3 (dBm)	-13

Table 5.20: UHF AT86RF215 Receiver characteristics

The minimum input signal that the AGC operates is calculated -81dBm as shown in figure 5.18(maximum gain of VGA).

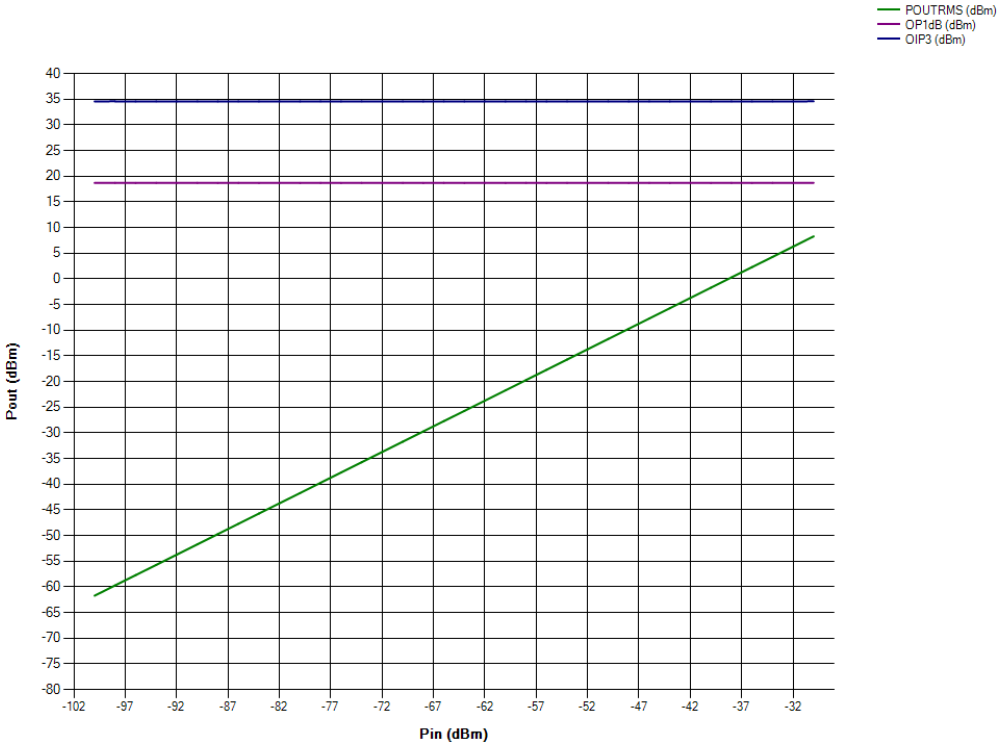

Figure 5.18: UHF Front-End Output Power

In order to design the resistive tap with coupling factor of -12dB, we use the impedance $173 - j430\Omega$ of AD8318 [37] at 450MHz. A Qucs simulation gives us the insertion loss (S21) and the coupling factor (S31) of the tap in figure 5.19. The P1 power source is the input of RF-mixer, P2 is the output of VGA and P3 is the detector input. The selected resistor for tap is ERA-2AEB820X [38] with 1% tolerance and temperature coefficient $25PPM/C$.

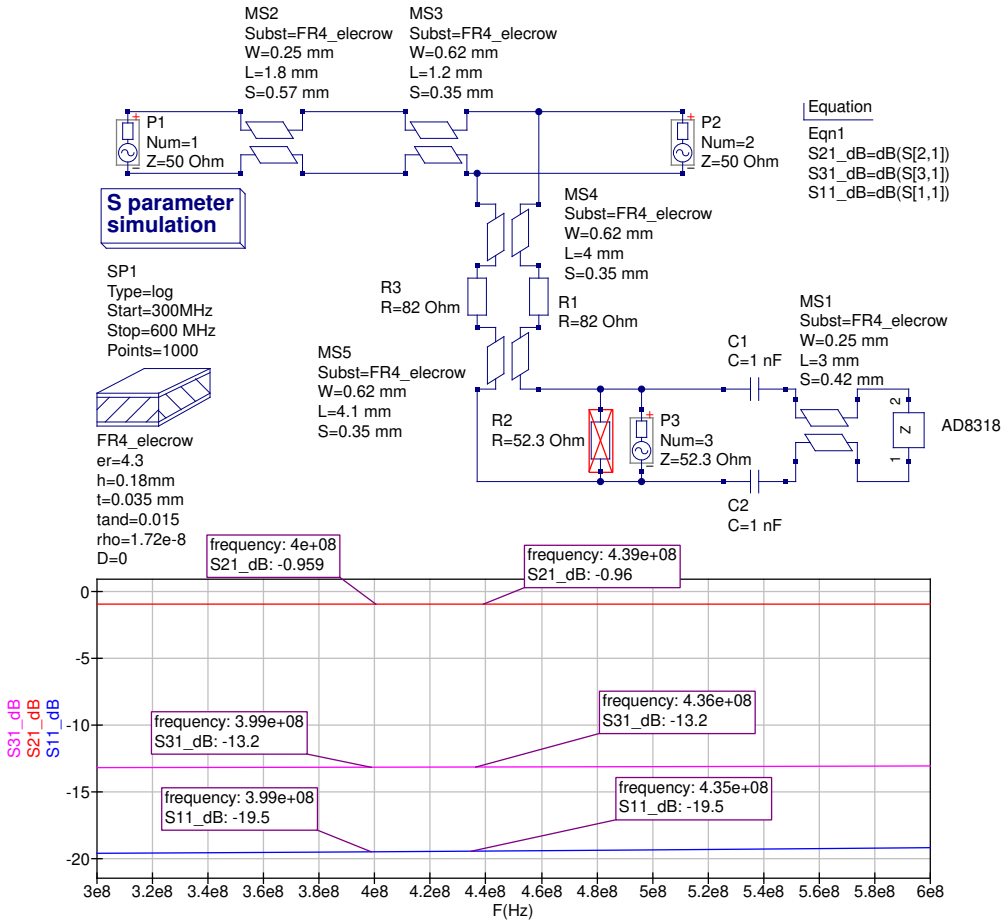

Figure 5.19: UHF Resistive Tap Coupling factor (S31) and Insertion Loss (S21)

The AGC protects the receiver from a strong signal that it could destroy components of the receiver like the transceiver which the absolute maximum RF input is +10dBm. Another import thing is to protect the receiver when the transmitter in enabled. The isolation of the RF-switch before the antenna must be at least -35dB. When the front-end transit signal of +30dBm in the input of receiver the signal level is -5dBm which is smaller than the maximum RF input of TQP3M9036[42] (+22dBm). An option for RF-switch before the antenna is F2972 [20], with typical isolation between common port and input ports is -48dB and low insertion losses of -0.4dB at 400MHz to 500MHz bandwidth. According to data-sheet of TQP3M9036[42] the OFF mode gain when the input signal is $(30 - 48) = -18dBm$ is -25dB, thus the output signal of LNA is -43dBm. By using the AGC and the wide bandwidth BPF, while the transmitter is enabled, the detector AD8318 could measure the output power which is useful in failure detection as described in Section 3.3.1. The control logic of UHF

receiver is designed in order to enable/disable every stage separately. The main load switch in figure 5.17 is control all the RX stages. Each of amplifiers and AGC are controlled by MCU via pins, AGC-EN and LNA-EN.

The radio, also supports transmission in UHF. As mention above:

- the LEO losses are 137–153dB
- the satellite antenna gain is 1.5dBi
- the ground station antenna is 16dBi

In order to calculate the minimum and maximum receiving signal, we defined at least 30dBm transmitting power of satellite, due to maximum available power of 8W and to low efficiency 35% (∼3.5W) of high linearity power amplifier. The receiving signal is -106.5dBm to -89.5dBm. As shown in table C.5 the (Eb/N0) margin for low elevations is negative due to high man-made noise (Antenna Noise Temp (k)) as described in Recommendation ITU-R P.372-14 [45].

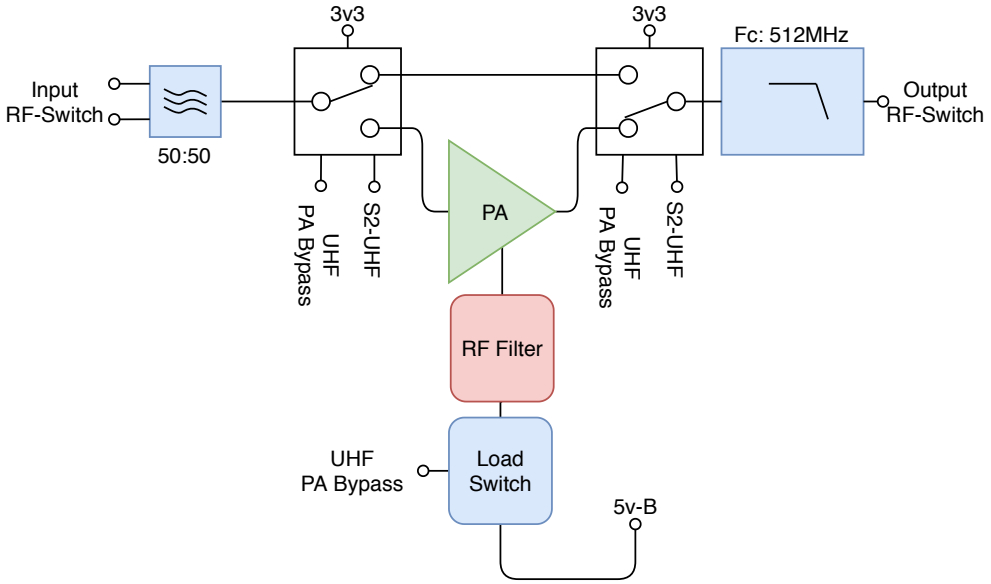

Figure 5.21: UHF Transmitter Front-End

The transmitter is appeared in figure 5.21. According to FCC-ID VW4A092353 [27] the AT86RF215 [1] development board is compliant with the SFCG 21–2R4 [26] recommendation 3 for low symbol rate spectral emission mask. In order the transmitter remains compatible with SFCG 21–2R4 [26] the AT86RF215 [1] harmonics (-30dBc 2nd harmonic, -14dBc 3rd harmonic) must be attenuated. Because of the balanced lines of AT86RF215 [1] a 1:1 balun is used, with part number ATB2012–50011-T000[44].

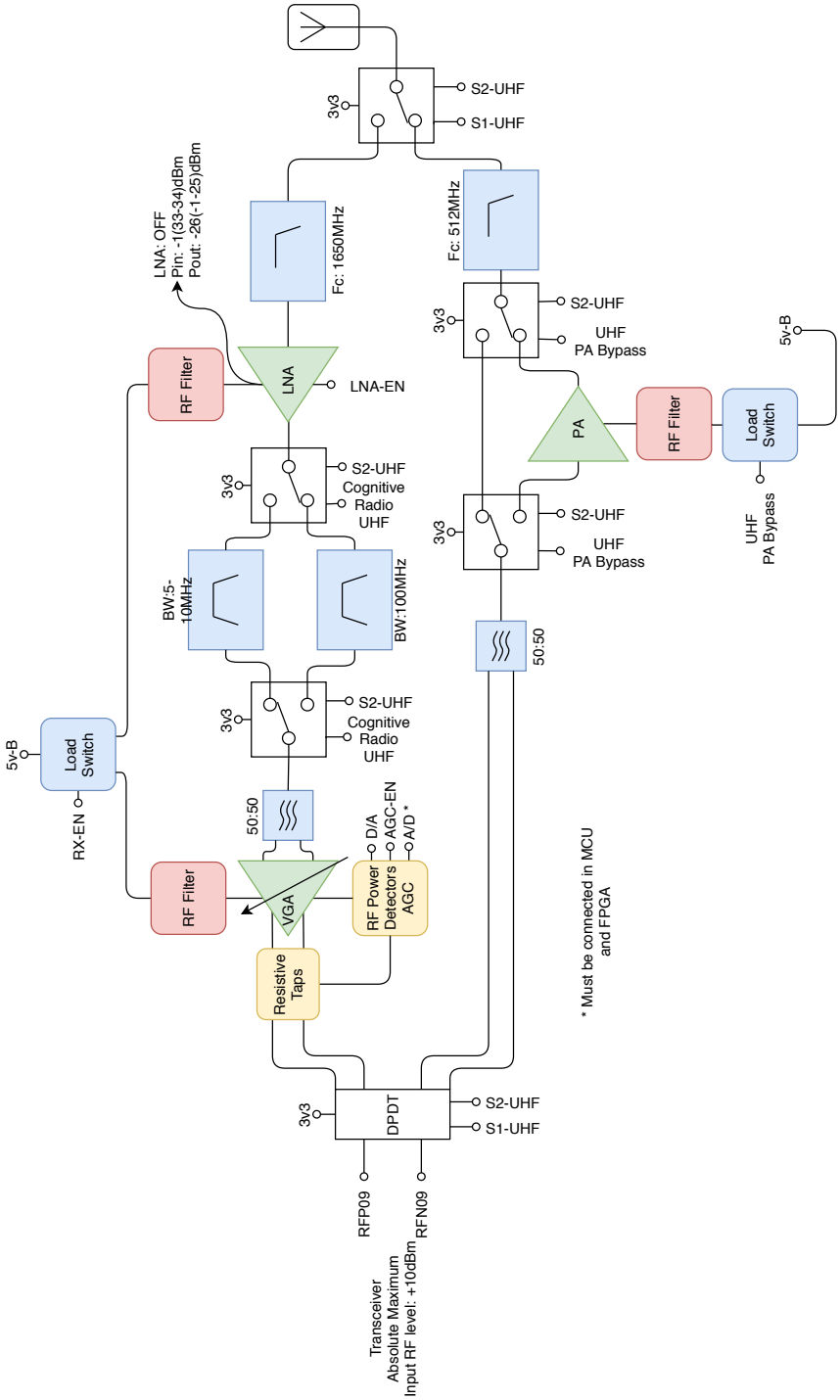

Figure 5.20: UHF Front-End

After the balun, the main amplifier and the recovery mechanism of it are followed. The RF-switches, as appeared in figure 5.21, are used to bypass the power amplifier when a failure is detected on it, as described in Section 3.3.1. An option for RF-switch is F2972 [20]. The same RF-switch is used before the antenna.

Component	DPDT	Balun	SPDT
Gain (dB)	-0.5	-1.5	-0.4
Noise Figure(dB)	0.5	1.5	0.4
IIP3(dBm)	55	2000	77
IP1dB (dBm)	24	2000	40
Bandwidth (MHz)	100-3000	40–860	5-10000
DC Power(mW)	0.0495	0	0.495
Part Number	SKY13421–486LF	ATB2012–50011–T0000	F2972

Table 5.21: UHF Transmitter Components — Part 1, Characteristics

According to table 5.21 and the with output power of AT86RF215 between +5dBm to +12dBm, the output power of signal after the first RF-switch is +2.6dBm to +9.6dBm. Before we define the gain of power amplifier, we must define the PAPR of supported modulations, table 5.22.

Modulation	PAPR (dB)
BPSK	3
MSK	3.3
FSK	TBD

Table 5.22: PAPR of Supported Modulations

It is necessary to amplify the signal in order to achieve a power output of +30dBm at least with peaks at +33dBm due to modulations. The output power is controlled by the internal VGA of AT86RF215 [1] with +1dB step. The frequency range of power amplifier must be 400MHz–450MHz. The gain of amplifier must be +23dB. An option of PA could be TQP7M9106 [46].

It remains to attenuate the harmonics of AT86RF215 [1] after the second RF-switch in order to be at least -60dBc as defined by SFCG 21–2R4 [26]. A low pass

filter (Fc:512MHz) is used as it is appeared in figure 5.21. An option could be the LFCG-490+ [40] with power handling of 3W. In the table 5.23 are presented the remaining components of transmitter.

Component	PA	SPDT	LPF	SPDT
Gain (dB)	25	-0.4	-1	-0.4
Noise Figure (dB)	N/A	0.4	1	0.4
IIP3 (dBm)	23.4	77	2000	77
IP1dB (dBm)	9	40	2000	40
Bandwidth (MHz)	400–500	5–10000		5–10000
Fc (MHz)	—	—	512	—
DC Power (mW)	3500	0.495	0	0.495
Part Number	TQP7M9106	F2972	LFCG-490+	F2972

Table 5.23: UHF Transmitter Components — Part 2, Characteristics

In figure 5.22 is presented the output power of front-end with various input from AT86RF215 [1].

Component	Transmitter
Gain (dB)	21.3
OP1dB (dBm)	29.5
OIP3 (dBm)	45.6

Table 5.24: UHF Transmitter cascade characteristics

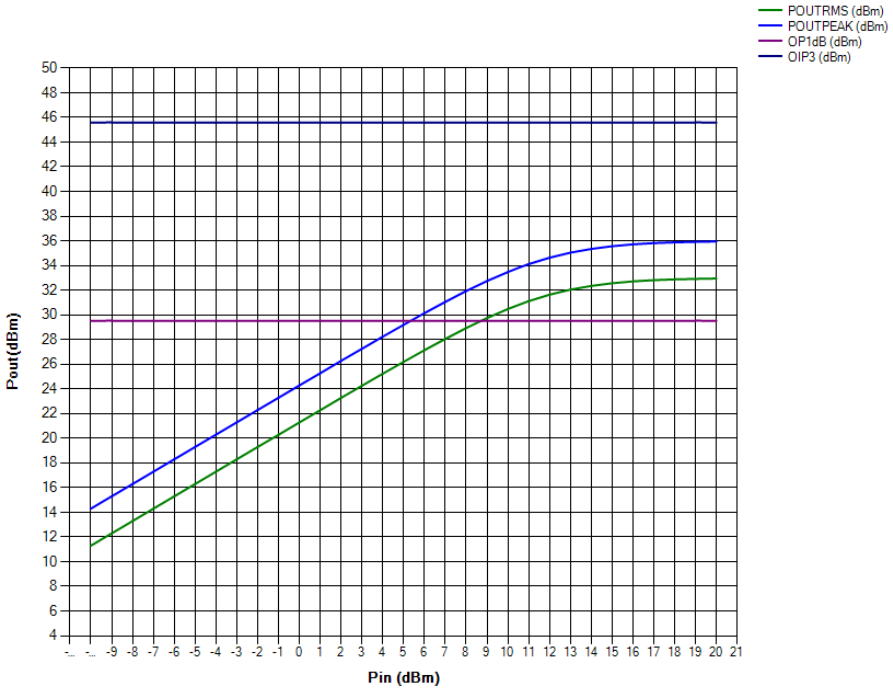

Figure 5.22: UHF Transmitter Output Power

In figures 5.23 and 5.24 are shown the TX chain and response of TX chain (in dB) and the input from AT86RF215 with harmonics (in dBm) which approves the compliance with SFCG 21–2R4 [26].

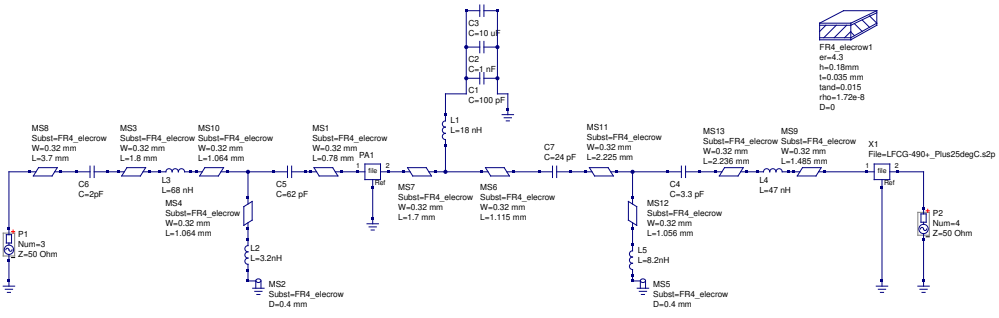

Figure 5.23: UHF Transmitter Chain

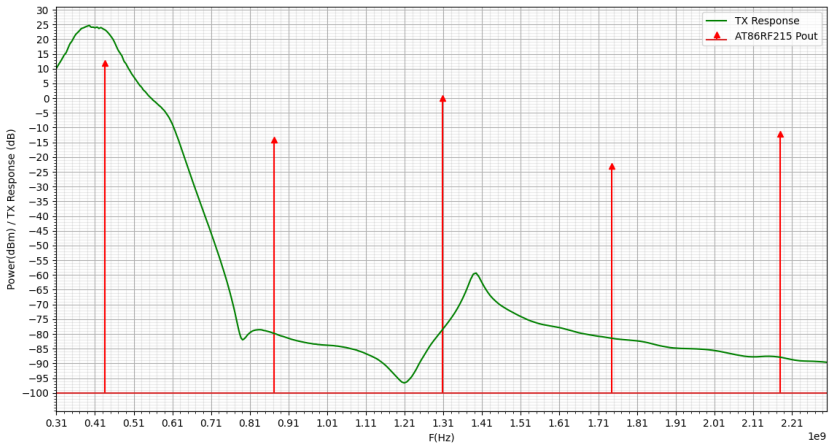

Figure 5.24: UHF Transmitter Response and AT86RF215 input

It is important to note that a worst case analysis for tolerances of sensitive passive components in PA matching is done in appendix G. The matching network it consist of a L-match and L-C in series as described in book RF Circuit Design [47]. In figure 5.25 is shown the simulation results of matching network.

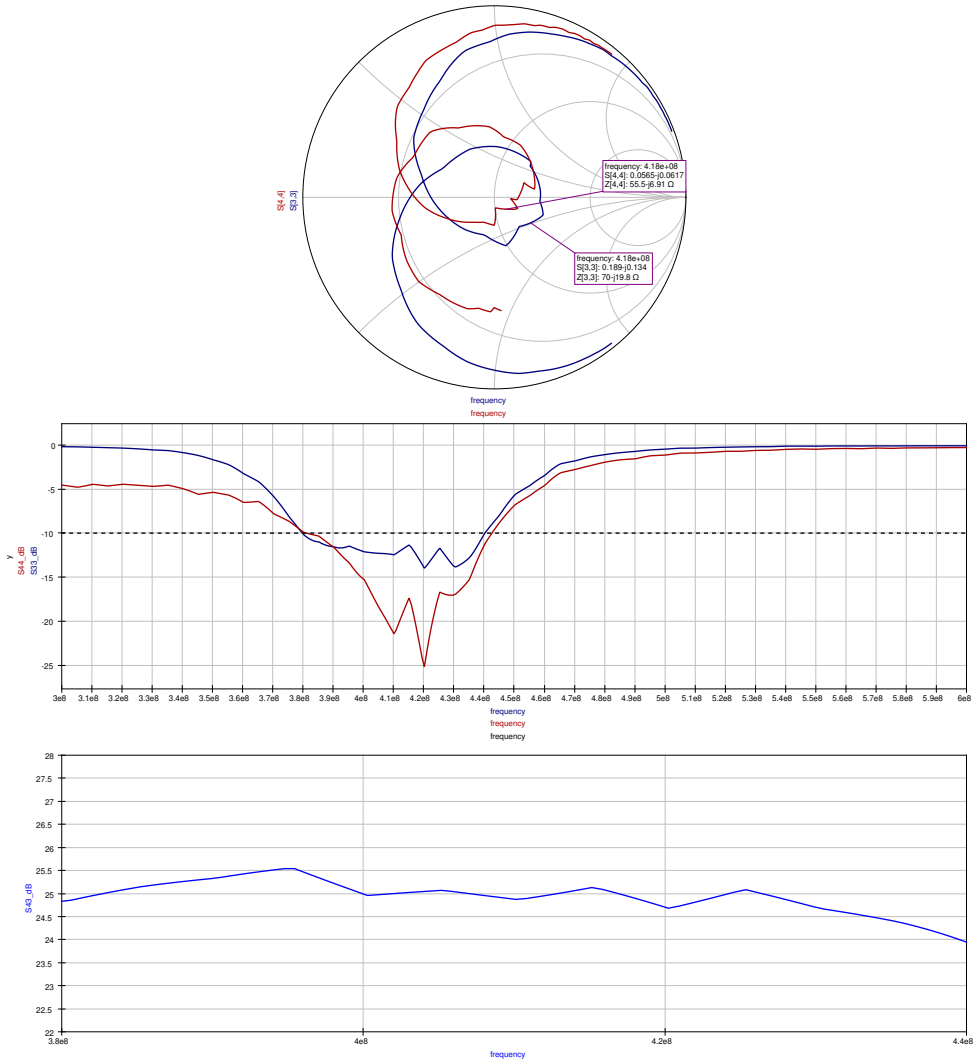

Figure 5.25: PA Matching network

Automatic Gain Control

The proposed AGC is a first order system that the loop bandwidth, as a result the time response, it depends on the capacitor C_{FLT}, as referred in AD8318 [37]. The detector AD8318 only loop bandwidth as referred in data-sheet is:

$$f_{3dB} = \frac{1}{\pi * 3.13k * (C_{FLT} + 1.5pF)} \tag{5.1}$$

When the AD8318 operates as controller the time constant T_0,

$$T_0 = \frac{V_{GBC}}{V_{SLP}} * T \tag{5.2}$$

Where:

- $T = \frac{1}{2*\pi*f_{3dB}}$ is time constant of detector
- V_{SLP}, represents the volts/decade of detector which is 0.48V/dB
- V_{GBC}, is the gain scaling of VGA that produced by the output power (dBm) as a function of control voltage (Typical Power-Control Curve). For 2200MHz (figure 12 of ADL5330 [36]) is 0.3V/dB and for 450MHz (figure 12 of ADL5330 [36]) is 0.4V/dB.

as described in AD8315 [48] data-sheet. An approximation (1_{st} order system) of attack and release is:

$$Attack/Release = 3 * T_0 \tag{5.3}$$

The estimation of attack/decay time by using different capacitors is presented in table 5.25.

Capacitor (pF)	Fc (MHz)	T_0 (us)	Attack/Release (us)
1000	2200	0.98	2.94
1000	450	1.31	3.92
470	2200	0.46	1.38
470	450	0.61	1.84
330	2200	0.32	0.97
330	450	0.43	1.30

Table 5.25: Estimated attack/release time of AGC by using different capacitors

In application note AN-1507 [35] does not exist any information related to the type of envelop.

Controller

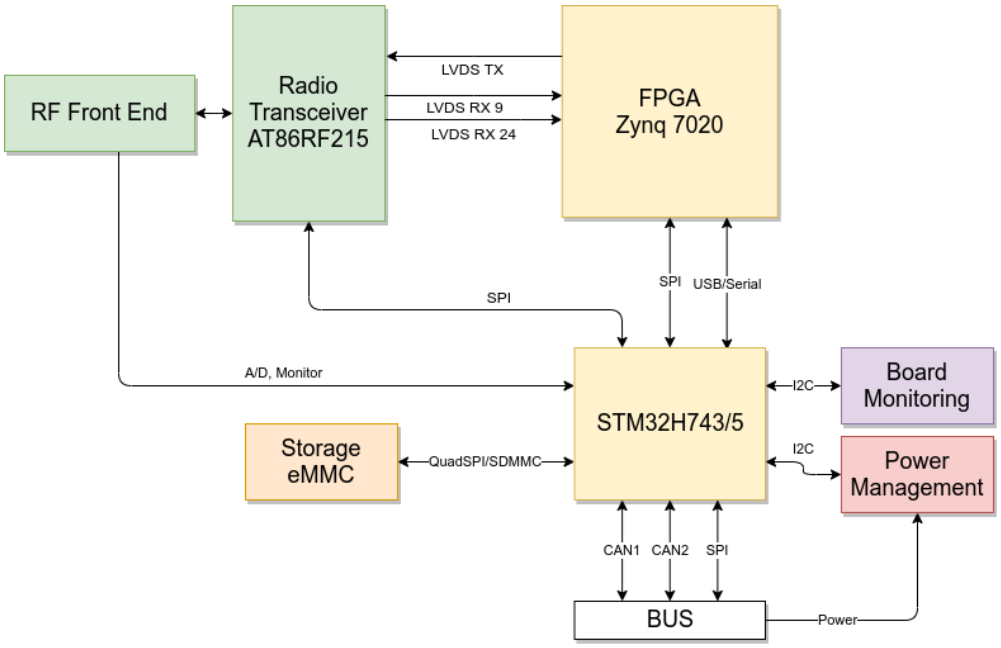

Figure 5.26: System blocks

For unit communication and control, the MCU uses 3 SPI buses for controlling the Digital Signal Processing unit, RF transceiver and for subsystem communication. Board temperatures are monitored using I2C bus and compatible I2C temperature sensors. Power monitoring comes from PMICs via I2C bus. On-board storage ICs used for store and forward operations and device reconfiguration are accessed through SDMMC interface. For subsystem communication two high speed CANFD interfaces and one SPI interface are used. An overview of MCU connection is shown in Figure 5.26

Board Monitor

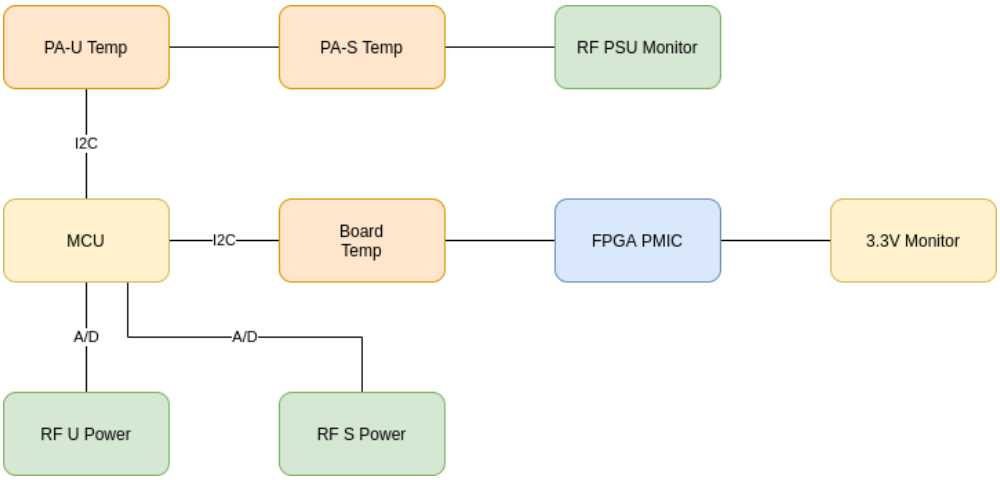

Figure 5.27: Board monitoring

Board power monitoring is provided by PMIC, 3.3V and 5V power monitors. Power information includes:

- Input voltage
- Output voltages per channel
- Current per channel
- Over-current events
- Over-current shutdown
- Over/Under voltage conditions
- PMIC temperature

Temperatures for power RF components are provided by dedicated temperature monitors positioned near these parts. RF power for each front-end is directly monitored by the MCU using ADC lines. Board power and temperature monitors communicate using two I2C buses as seen in Figure 5.27

Power Distribution

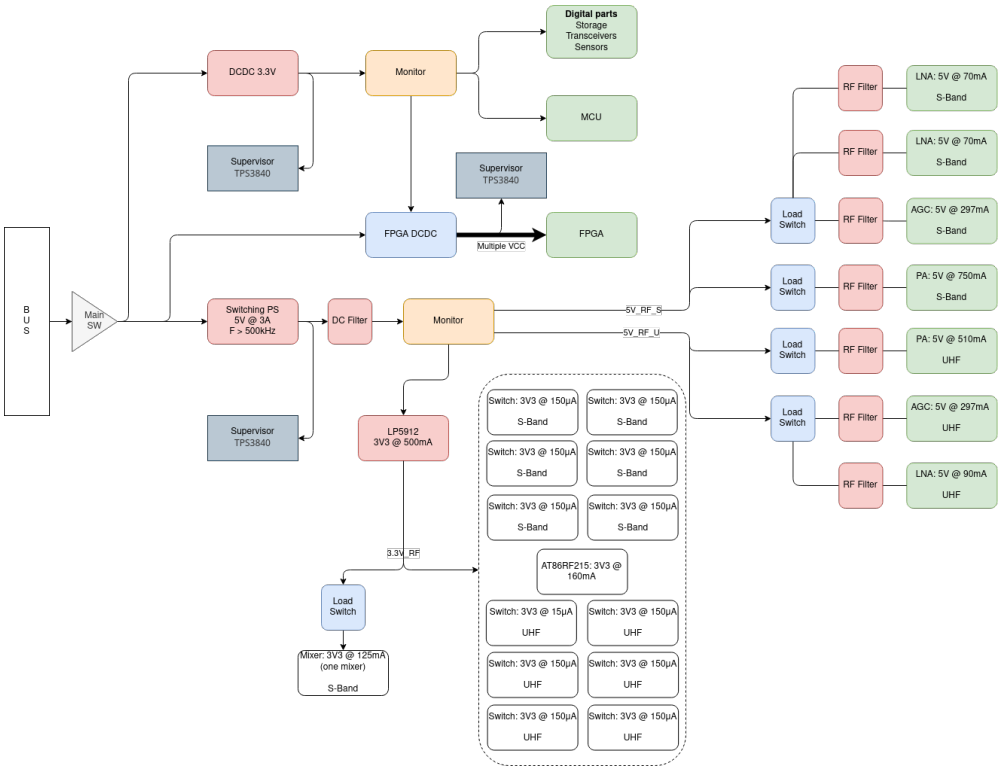

Figure 5.28: Power distribution

Power supply circuit is build around IRPS5401 PMIC for FPGA and two DC-DC converters for digital and RF parts. Low noise RF parts are power via 3.3V LDOs to minimize interference. Power to each RF section is controlled by a load switch. RF power consumption is monitored via the 5V power monitor while digital parts power is monitored by 3.3V power monitor. Distribution path is shown in Figure 5.28. During operation PMIC DC-DC outputs are controlled and monitored by the MCU via I2C bus. Also each load switch (FPF2701 [49]) it has a current limit sensing that is regulated by a external resistor as shown in table 5.26. The FPF2071 responds to an overload condition that lasts longer than a fixed blanking period by latching off the load and pull down the pin FLAGB. The load remains off unless either the ON pin is toggled or the input voltage cycles through under voltage lock out.

Load Switch	Rset(Ω)	Current Limit (mA - typ.)
RF - Mixer	549k	510
RX - S-Band	110k	2500
TX - S-Band	110k	2500
RX - UHF	374k	740
TX - UHF	110k	2500

Table 5.26: Load switch current limit

The above mechanism is used by fault detection, isolation and recovery as described in section 3.3.1.

Since PMIC are fully programmable and initial outputs depend on OTP registers, there is a need to mitigate corruption of register content, although corruption must occur in multiple bits and in a way that produces an over-voltage condition. Initially all outputs are disabled, MCU validates register content and enables outputs. During operation OTP memory and registers are monitored and refreshed by MCU.

For overall system protection from latch events, all power outputs are monitored by hardware supervisors. If a MOSFET is latched leading to over-voltage condition, power to all DCDC converters is cycled from Main Power Switch resetting all MOSFETS.

Power consumption estimations

Based on component documentation, maximum power consumption for each mode is displayed in Table 5.27 as well as the absolute maximum power consumption. Final values are expected to be lower as consumption will vary based on RF Modulation scheme and software optimizations of MCU and FPGA

Board Layout

A preliminary component placement is shown in Figure 5.29 and Figure 5.30 while the most recent version of schematic and PCB layout are available in the project repository [15] and can also can be viewed online on CADLab [50]

Component	Amax	V	Efficiency	Pmax	P Tx U	P Rx U	P Tx S	P Rx S
Mixer	155.00 mA	3.30 V	61%	841.28 mW			841.28 mW	841.28 mW
RF switch	1.00 mA	3.30 V	61%	5.43 mW			5.43 mW	5.43 mW
RF switch	1.00 mA	3.30 V	61%	5.43 mW	5.43 mW	5.43 mW		
RF switch	1.00 mA	3.30 V	61%	5.43 mW			5.43 mW	5.43 mW
RF switch	1.00 mA	3.30 V	61%	5.43 mW			5.43 mW	
RF switch	1.00 mA	3.30 V	61%	5.43 mW			5.43 mW	
RF switch	1.00 mA	3.30 V	61%	5.43 mW				5.43 mW
RF switch	1.00 mA	3.30 V	61%	5.43 mW				5.43 mW
RF switch	1.00 mA	3.30 V	61%	5.43 mW	5.43 mW	5.43 mW		
RF switch	1.00 mA	3.30 V	61%	5.43 mW	5.43 mW			
RF switch	1.00 mA	3.30 V	61%	5.43 mW	5.43 mW			
RF switch	1.00 mA	3.30 V	61%	5.43 mW		5.43 mW		
RF switch	1.00 mA	3.30 V	61%	5.43 mW		5.43 mW		
VGA-S	300.00 mA	5.00 V	95%	1578.95 mW			1578.95 mW	1578.95 mW
AGC-S	0.00 mA	5.00 V	95%	0.00 mW			0.00 mW	0.00 mW
LNA2-S	52.00 mA	5.00 V	95%	273.68 mW			273.68 mW	273.68 mW
LNA1-S	52.00 mA	5.00 V	95%	273.68 mW				273.68 mW
PA-S	1050.00 mA	5.00 V	95%	5526.32 mW			5526.32 mW	
LNA-U	72.00 mA	5.00 V	95%	378.95 mW		378.95 mW		
VGA-U	300.00 mA	5.00 V	95%	1578.95 mW	1578.95 mW	1578.95 mW		
AGC-U	0.00 mA	5.00 V	95%	0.00 mW	0.00 mW	0.00 mW		
PA-U	693.00 mA	5.00 V	95%	3647.37 mW	3647.37 mW			
STM	119.00 mA	3.30 V	94%	417.77 mW	417.77 mW	417.77 mW	417.77 mW	417.77 mW
Transceiver	85.00 mA	3.30 V	61%	461.35 mW	230.67 mW	92.40 mW	230.67 mW	92.40 mW
FPGA			75%	1812.00 mW	1812.00 mW	1812.00 mW	1812.00 mW	1812.00 mW
eMMC	200.00 mA	3.30 V	94%	702.13 mW	702.13 mW	702.13 mW	702.13 mW	702.13 mW
T Sensor	0.20 mA	3.30 V	94%	0.70 mW	0.70 mW	0.70 mW	0.70 mW	0.70 mW
T Sensor	0.20 mA	3.30 V	94%	0.70 mW	0.70 mW	0.70 mW	0.70 mW	0.70 mW
T Sensor	0.20 mA	3.30 V	94%	0.70 mW	0.70 mW	0.70 mW	0.70 mW	0.70 mW
DDR			75%	800.00 mW	800.00 mW	800.00 mW	800.00 mW	800.00 mW
DDR			75%	800.00 mW	800.00 mW	800.00 mW	800.00 mW	800.00 mW
CAN transceiver	60.00 mA	3.30 V	94%	210.64 mW	210.64 mW	210.64 mW	210.64 mW	210.64 mW
CAN transceiver	60.00 mA	3.30 V	94%	210.64 mW	210.64 mW	210.64 mW	210.64 mW	210.64 mW
Total power								
				19.58 W	10.43 W	7.03 W	13.43 W	8.04 W

Table 5.27: Analytic power consumption table

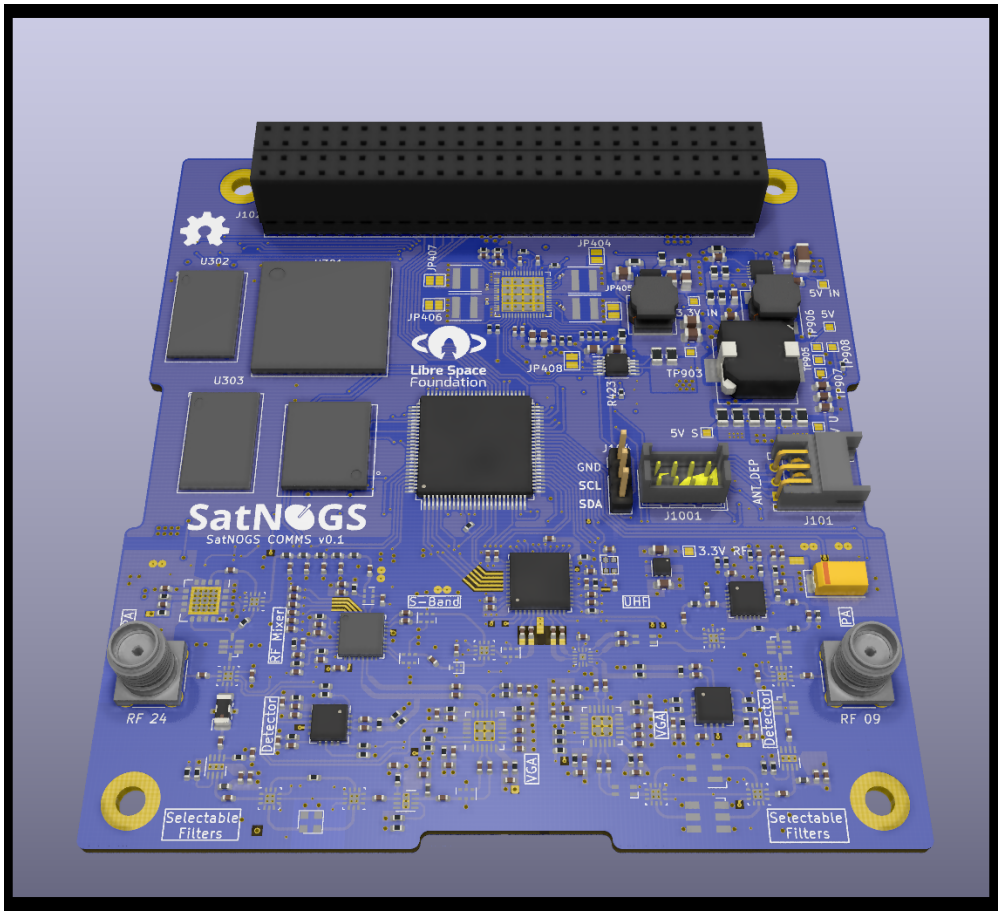

Figure 5.29: PCB Top side

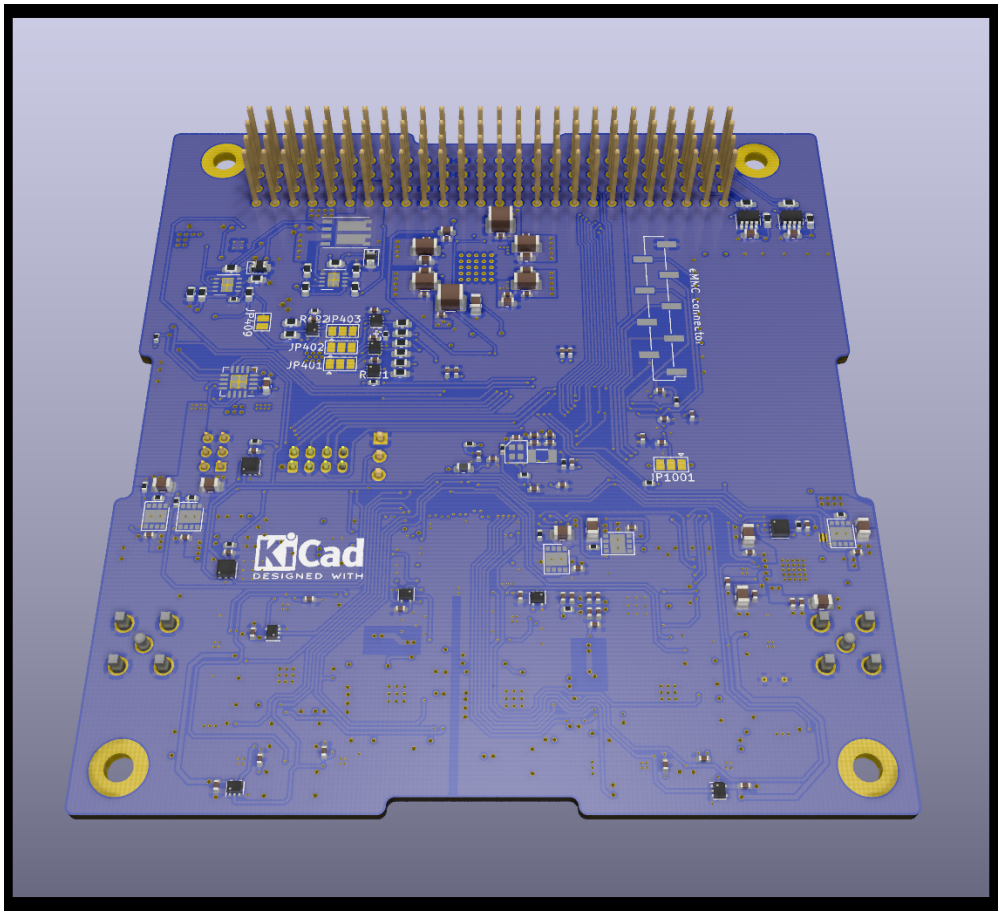

Figure 5.30: PCB Bottom side

Derating

Since COTS components not fall under ECSS-Q-ST-60, ECSS-Q-ST-30-11C Rev 1 is not applied as per ECSS-Q-ST-30-11C 5.3.1

Nonetheless, component selection and operating envelope will be based on ECSS-Q-ST-30-11C where possible.

Component operating voltages shall be chosen based on over-voltage monitor reaction time, DCDC converter voltage rise rate and component thresholds based on the following formula:

$$V_{\min} < VCC_{\max} < \frac{V_{\max} - V_{Slope} \cdot t_{PD}}{1 + T_{threshold}}$$

Using the formula above, maximum VCC for power rails are shown in Table 5.28

and Table 5.29

$\mathbf{V_{slope}}$	$\mathbf{T_{threshold}}$	$\mathbf{t_{PD}}$
2.50 V/ms	4.00%	$30\mu s$
Rail	$\mathbf{V_{max}}$	$\mathbf{VCC_{max}}$
1V	1.1	0.985
1.8V	2	1.850

Table 5.28: PMIC Power rail maximum VCC

$\mathbf{V_{slope}}$	$\mathbf{T_{threshold}}$	$\mathbf{t_{PD}}$
0.88 V/ms	5.00%	$0.6\mu s$
Rail	$\mathbf{V_{max}}$	$\mathbf{VCC_{max}}$
3.3V	3.6V	3.428V
5V	5.5V	5.237V

Table 5.29: DCDC Power rail maximum VCC

5.1.2 Software

DSP Software

The ground segment uses the SDR technology to perform the DSP tasks. The software runs on any general purpose CPU using the GNU Radio as the base platform. On top of GNU Radio, several modules are used to extend the basic functionality of the platform. The overall architecture is depicted in Figure 5.31.

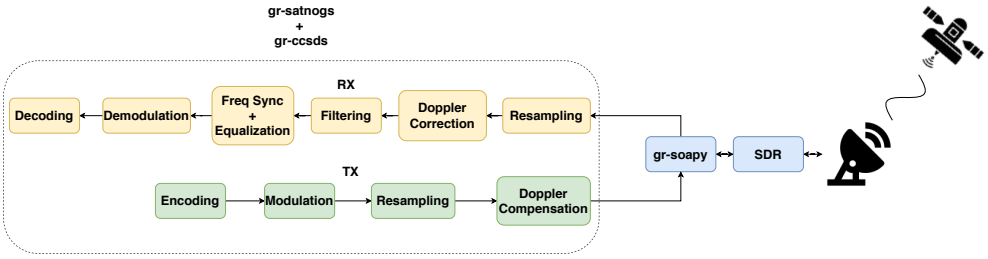

Figure 5.31: DSP software operations at the ground segment

The gr-soapy [51] is a GNU Radio that wraps the SoapySDR [52] library. This module provides a unified and vendor neutral way to access and configure a wide range of different SDR devices. This module increases the flexibility of the ground station and allows more robust and unified implementation of the DSP software.

For the processing of the digital I/Q samples, the gr-satnogs [4] and the gr-ccsds [53] GNU Radio modules are used. The gr-satnogs is responsible for common DSP tasks vital for satellite communications. During reception, it re-samples the received I/Q stream. This is done for two main reasons. The first one is that different SDR front-ends have different sampling rate tune-ability capabilities. The second one, has to do with the computational resources required for the DSP tasks. By properly re-sampling the signal to lower sampling rates, DSP tasks that follow will require less computational resources. This is an approach already tested in the SatNOGS Network with great success, allowing the ground station to operate even in SBCs, like the Raspberry Pi. This gives a great advantage on the ground station, in terms of flexibility, acquisition and maintenance cost. After re-sampling, gr-satnogs performs Doppler frequency correction. Because the ground station should be able to operate with both suppressed and residual carrier modulation schemes, the Doppler frequency offset is mainly corrected using the orbital information of the satellite provided by its TLE. However, the reception processing chain after some filtering, tries to compensate any remaining frequency offset and equalize the signal amplitude to a reference level, in order to maximize the performance of the demodulator. Based on the transmitter characteristics, the ground station utilizes one of the available modulation, coding and framing schemes provided by gr-satnogs, in order to demodulate and decode the received frames. In addition, the gr-ccsds module provides a set of transceivers implementing the CCSDS recommendations for telemetry and telecommand synchronization and channel coding. The implementation follows the specifications for Category A spacecrafts, described in the CCSDS blue books CCSDS 131.0-B-3, CCSDS 231.0-B-3 and CCSDS 401.0-B-28.

During transmission, the ground station uses the corresponding processing blocks provided by gr-satnogs and gr-ccsds in order to construct the digital signal. Before propagating the samples to the SDR front-end, the ground station inserts properly a frequency shift that will compensate the shift due to the Doppler as it will be observed from the spacecraft perspective. This greatly eliminates the complexity of the receiver at the space segment.

At the SatNOGS COMMS transceiver a similar approach is used. The integrated modem of the AT86RF215 IC does not support all of the required modulation, coding and framing schemes. This modem is still available to use it on demand, in case low power consummation is necessary. Using the integrated modem, the FPGA is powered down and transceiver operations are accomplished only with the MCU intervention. However, on this operational mode only suppressed carrier modulations are available. Any frequency offset is handled by the internal frequency offset compensation mechanism of the hardware modem.

On the other hand, using the I/Q interface and the on-board FPGA all the necessary DSP tasks can be implemented on software. On this mode, all of the required CCSDS modulation and coding schemes are supported. In addition, phase modulation with residual carrier is available with a configurable modulation index and a set of user-selectable line coding options (NRZ-M, NRZ-L, SP-L) for both TX and RX operations. The Digital Signal Processing (DSP) software required for the I/Q mode executes on the ZYNQ-7020 FPGA. The time critical and processing intensive operations (AGC, frequency recovery, clock recovery, FEC decoding) are implemented on

the FPGA. To offload the FPGA, some of the less time critical operations, like frame handling, CRC checks are implemented on the Dual-Core ARM Cortex-A9 processor generic processor of the ZYNQ-7020.

5.1.3 Telecommand and Control

For the TMTC, the SatNOGS COMMS uses the OSDLP [11] library. This software package implements the CCSDS Space Packet [54] and the CCSDS Data Link protocol for TM [55] and TC [56]. This library is implemented in an OS-independent fashion, therefore the same implementation is used on board the transceiver and at the ground station. Figure 5.32 and Figure 5.33 depict the TMTC packet format.

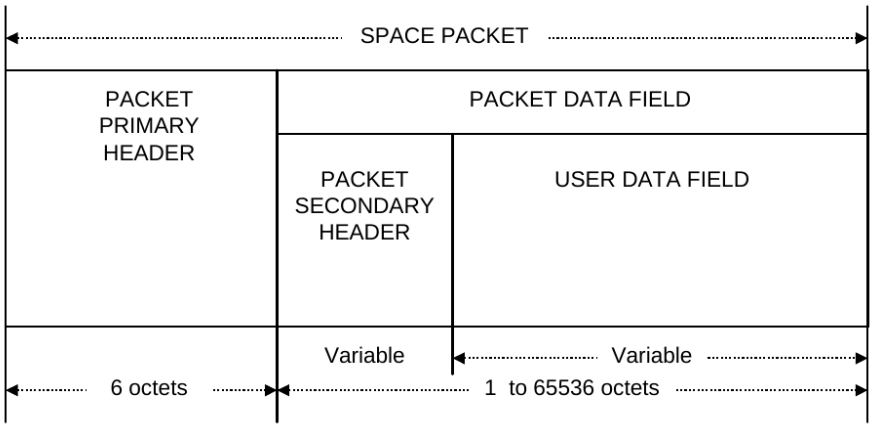

Figure 5.32: CCSDS Space Packet Structural Components

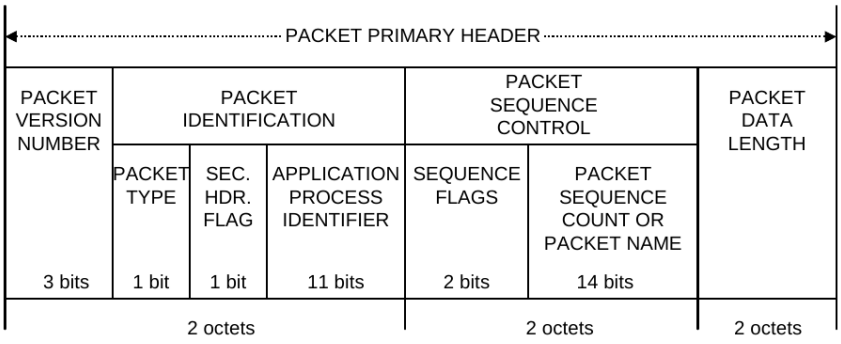

Figure 5.33: CCSDS Space Packet Primary Header

Ground Segment Subsystems

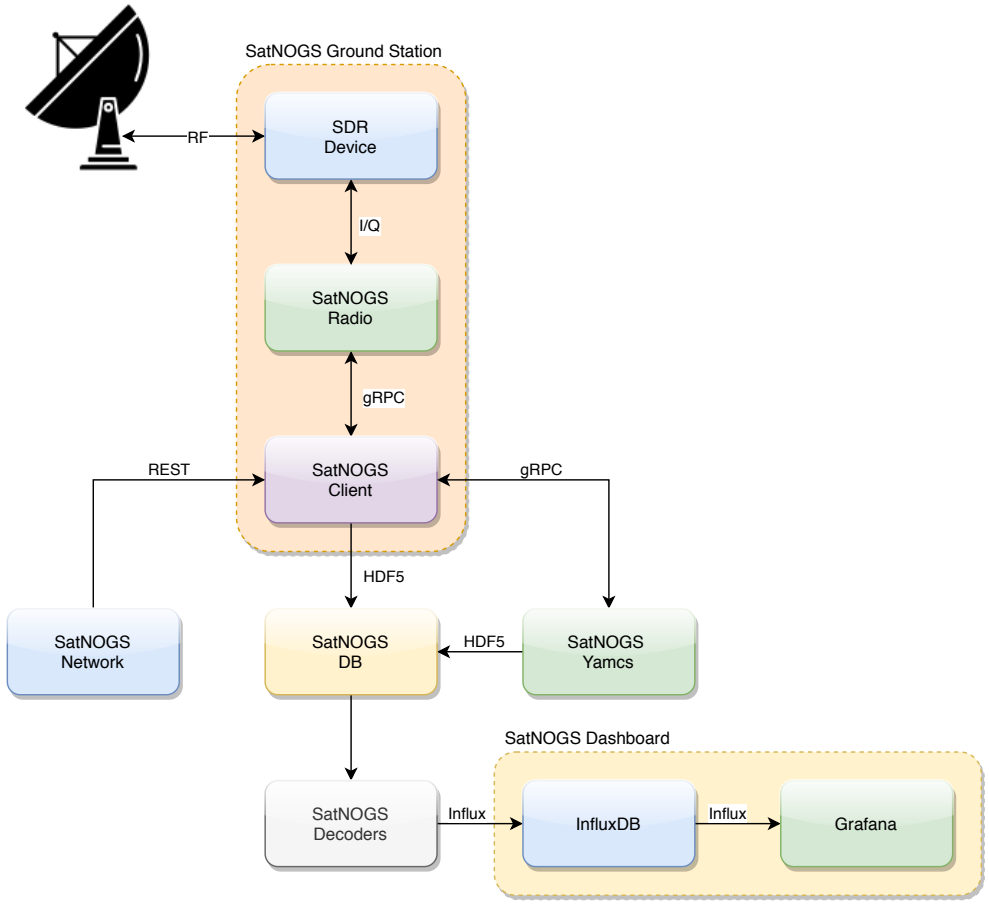

Figure 5.34: Ground Segment Subsystems

The Ground Segment Subsystems is a set of independent subsystems which interact to provide telemetry and telecommand services. Figure 5.34 shows a diagram of the these subsystems. The SatNOGS Ground Station comprises of the Software Defined Radio device, the SatNOGS Radio which is the software implementation of the DSP describe above, and the SatNOGS Client which is the controlling software. A gRPC interface is used for the communication of the client and the radio to provide high-performance RPC calls and bidirectional streaming. The client periodically pulls jobs (called 'Observations') from SatNOGS Network through a REST API which the network provides. These jobs reserve the time of the ground station for operations and are scheduled based on operator's selection and algorithms which calculate spacecraft

passes.

There are two modes of operation for receiving telemetry; non real-time and real-time. On non real-time mode, the client packs all telemetry data along with any other information and metadata of the Observation within an HDF5 file, and sends them directly to SatNOGS DB through a REST API. On real-time mode, the client opens a gRPC connection with the SatNOGS Yamcs server. The Yamcs server is a fully featured mission control framework which is properly customized to meet the requirements of the operator and receives the telemetry, processes it, stores it and makes it available to any user interface through its own API. Once the telemetry reaches Yamcs and is processed, it is further forwarded to SatNOGS DB for archival and visualization purposes.

When operating in telecommand mode, a similar gRPC connection is also established between the client and Yamcs. Again, Yamcs is customized to support the operators requested commands. Since the connection is initiated by the client, handover from ground station to ground station is controlled by SatNOGS Network based on calculated scheduling time-slots.

Further down the pipeline, telemetry data reaching SatNOGS DB are processed with telemetry decoders and stored in a InfluxDB time series database. A Grafana instance is then used to visualize this data. Grafana Dashboards are developed and customized based on satellite operator's requirements.

QA Testing

The SatNOGS COMMS software and hardware components are tested using the hardware in the loop approach depicted in Figure 5.35. Using the techniques provided by the SDR Testbed [57] project, a hardware simulation setup constantly tests all the affected components emulating a ground station communicating with a satellite equipped with the SatNOGS COMMS transceiver. To do so a SBC computer running all the required ground station software components is used. The SBC is responsible to modulate and demodulate the baseband digital signal. During uplink, the digital signal is fed to the gr-leo [30] GNU Radio module. This module emulates a dynamic satellite channel. It introduces path loss, Doppler frequency shift as well as other type of attenuation, like rainfall, gas, and/or pointing loss. The digital signal with the LEO channel impairments, is transmitted using an SDR device with the help of the gr-soapy [51] module. The resulting RF signal is fed into a network of attenuators and RF switches. The programmable alternators introduce extra attenuation if necessary, whereas the RF-switches select the appropriate signal paths, based on the band of interest. The same approach is used for downlink testing too. Throughout the QA testing session, both the ground station as well as the SatNOGS transceiver, produce logs with the performance of their receivers.

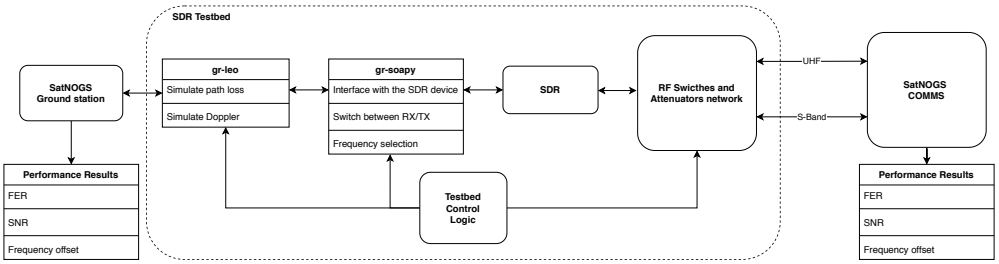

Figure 5.35: QA testing with hardware in the loop

6. Interfaces

6.1 Mechanical interface

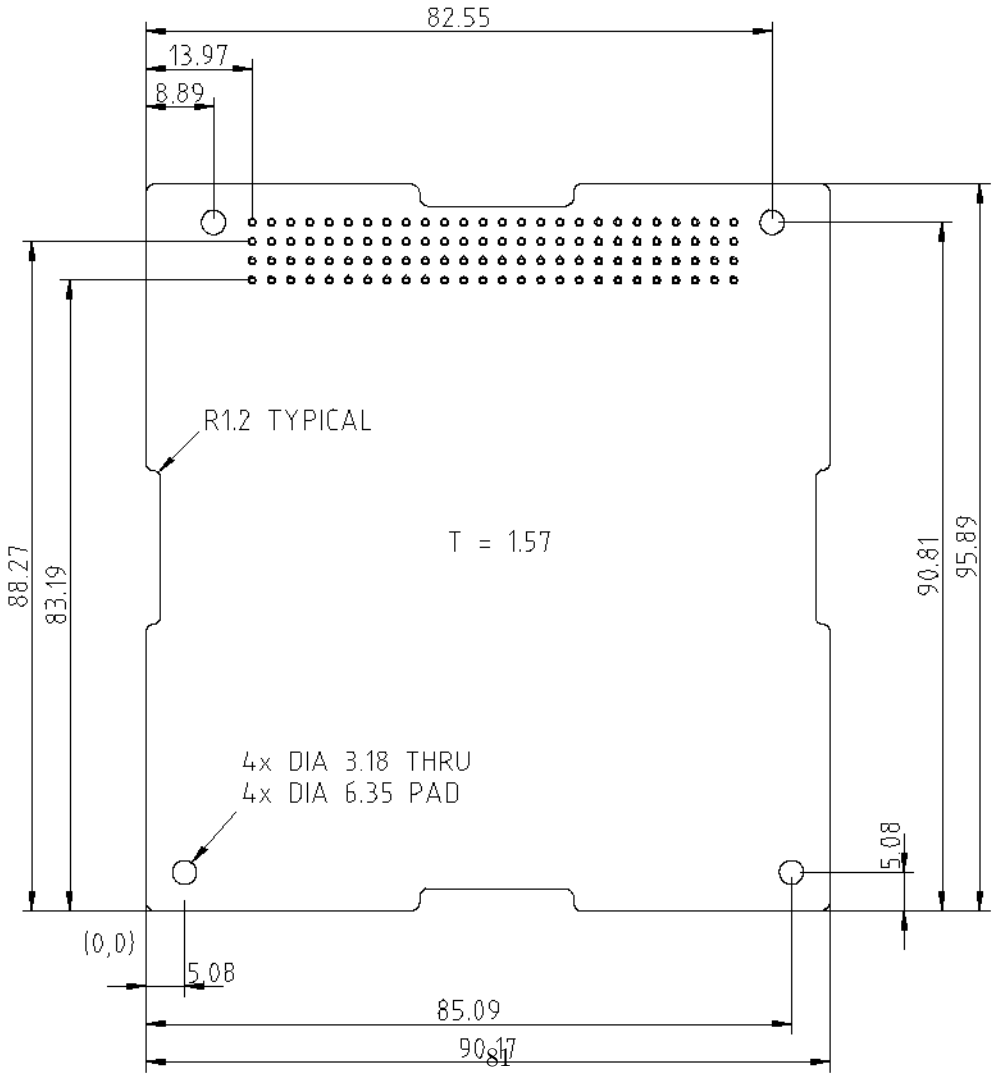

Figure 6.1: LibreCube mechanical drawing (dimensions in mm)

PCB dimensions, mounting holes, connector type and location follow LibreCube [58] standard. Interface connectors are SAMTEC ESQ-126–39–G-D. Mechanical drawing is shown in Figure 6.1

6.2 Subsystem interface

For subsystem communication the following interfaces are available:

- Two CAN-FD interfaces backward compatible with CAN-2.0
- SPI Interface having maximum link speed of 8Mbps

CAN-FD fulfills interconnect link speed requirements. Subsystems only capable of CAN-2.0 can use SPI for data transfer and CAN-2.0 for control.

RF connectors will be either SMA or MCX

6.2.1 Antenna deployment

Antenna deployment interface exposes two closed loop control endpoints. Each endpoint consists of control signal and detection signal lines exposed via a Hirose DF11–8DP-2DS (52) with option of Hirose DF11–8DP-2DSA (01). Additionally these lines can be available on the main connector.

Control signal lines are software configurable as either 3.3V Push-Pull or Open-Drain. Maximum input voltage in Open-Drain configuration is restricted to 5V by protection diode. Control signal current is limited to 18mA via 270Ω resistor

Detection signal lines are 3.3V compatible and software configured as Pull-Up, Pull-Down or Floating. Pull-Up and Pull-Down resistor value is $40k\Omega \pm 10k\Omega$. Each detection line is protected from over-voltage via 3.3V Zener diode and 330Ω resistor.

Electrical connection of signal lines is provided via an 8 pin connector as shown in Figure 6.2

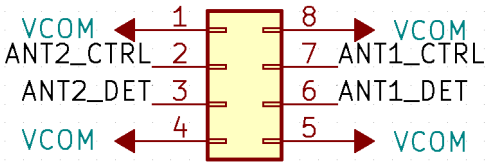

Figure 6.2: Antenna Control Connector

6.2.2 Power supply

COMMS transceiver accepts an input voltage range varying from 6V DC to 14V DC. Absolute maximum power consumption is estimated at 20W. This value should never be reached under normal operating conditions.

6.3 Ground Segment

6.3.1 Telemetry API

SatNOGS provides an API for receiving acquired telemetry as well as signal acquisition parameters. For non real-time operation, raw telemetry data is uploaded directly to SatNOGS DB servers by SatNOGS Client, on predefined intervals. This API endpoint accepts HDF5 formatted files which include additional information and metadata of the scheduled SatNOGS Network observation. The telemetry data are then processed and forward to the InfluxDB database of SatNOGS Dashboards in order to be visualized. For real-time operation, SatNOGS Client forwards the telemetry data to a SatNOGS Yamcs server. The SatNOGS Yamcs server receives the data through a data link plugin which provides a gRPC interface for telemetry. In this case, telemetry data is still eventually forwarded to SatNOGS DB via the Yamcs server and a SatNOGS DB API data link plugin.

6.3.2 Telecommand API

SatNOGS provides an API allowing telecommand data transmission. SatNOGS Client gRPC interface is used to receive telecommands. These commands are sent by the SatNOGS Yamcs server via a gRPC data link plugin. The client then forwards the telecommands to SatNOGS Radio in order to be encoded and transmitted via the SDR.

7. Requirements Matrix

REQ	Section	Compliance	Comment
-006	6.2	Full	
-007	6.1	Full	
-008	6.1	Full	
-009	—	TBD	
-010	—	TBD	
-013	5.1.2	Full	
-015	6.2.1	Full	
-017	6.2.2	Partial	The IRPS5401 PMIC, nominal input voltage range is 6 — 14 V
-018	6.2	Full	
-019	5.1.1	Full	
-020	5.1.1	Full	
-021	5.1.1	Partial	The AT86RF215 [1] integrated transceiver does not support concurrent operation in I/Q mode due to the single LVDS interface.
-022	5.1.1	Full	
-026	5.1.1	Full	
-027	6.3	Full	
-029	5.1.1	Full	
-030	—	TBD	
-031	—	TBD	
-032	—	TBD	
-033	—	TBD	
-034	—	TBD	
-035	—	TBD	
-036	—	TBD	
-037	—	TBD	
-038	—	TBD	
-039	5.1.1	Full	
-040	5.1.1	Full	
-041	5.1.1	Full	
-042	—	TBD	
-043	—	TBD	
-045	5.1.3	Full	
-046	5.1.3	Full	
-049	—	TBD	
-050	—	TBD	
-051	—	TBD	

-052	—	TBD	
-053	—	TBD	
-054	—	TBD	
-055	—	TBD	
-056	—	TBD	
-057	—	TBD	
-058	—	TBD	
-059	—	TBD	
-061	5.1.1	Full	
-062	6.2.1	Full	
-063	—	TBD	
-064	6.3.1	Full	
-065	6.3.2	Full	
-066	—	TBD	
-067	—	TBD	
-068	—	TBD	
-070	5.1.2	Full	
-071	5.1.2	Full	
-072	—	TBD	
-073	5.1.2	Full	
-074	—	TBD	
-075	5.1.3	Full	
-076	—	TBD	
-078	—	TBD	
-079	—	TBD	
-080	—	TBD	
-081	—	TBD	
-082	—	TBD	
-083	—	TBD	
-084	5.1.1	Full	
-085	—	TBD	
-086	—	TBD	
-087	—	TBD	
-088	—	TBD	
-089	—	TBD	
-090	—	TBD	
-091	—	TBD	
-092	—	TBD	
-136	5.1.1	Full	
-137	5.1.1	Full	
-138	—	TBD	
-139	—	TBD	
-140	5.1.1	Full	
-142	5.1.2	Full	
-143	5.1.2	Full	
-144	—	TBD	
-145	6.2.2	Full	
-146	6.2.2	Full	
-147	6.2.2	Full	
-148	6.2.2	Full	
-149	—	TBD	
-150	—	TBD	
-151	6.2.1	Full	

-152	—	TBD	
-153	—	TBD	

Appendices

A. Interfaces Data Sheet

INTERFACE DATA SHEET				
	I/F Designation:	**DC Power interface**		
ID	**Source Circuit Specification**		Ver	Iss
-1	Bus voltage	6V-14V input range		
-2	Bus current	1.6A max @ 14V Bus voltage 3.5A max @ 6V Bus voltage		
-3	Response to bus undervoltage	All loads except MCU switch off automatically MCU is deactivated at 3.2V Bus voltage		
-4	Bus voltage (anomaly):	The load shall not be damaged when subjected to any bus voltage in the range 0V to 14V, steady-state or at any rate of change.		

Table A.1: DC Power Interface characteristics

INTERFACE DATA SHEET				
	I/F Designation:	**SPI interface**		
ID	**Voltage, data rate and timing specification**		Ver	Iss
-1	Data rate	8 Mbps for 3m total bus length between devices		
-2	Voltage range	0V–3.3V		
-3	Voltage tolerance	-0.3V–5.5V		
-4	SPI clock frequency	Slave receiver mode: 100MHz max Slave mode transmitter/full duplex: 31MHz Slave mode transmitter/full duplex: 25MHz		
-5	NSS setup time	Min 2ns		
-6	NSS hold time	Min 1ns		
-7	Data input setup time	Min 2ns		
-8	Data input hold time	Min 1ns		
-9	Data input hold time	1ns		
-10	Data output access time	9ns–27ns		
-11	Data output disable time	Max 5ns		
-12	Data output valid time	Max 16ns		
-13	Data output hold time	Min 9ns		

Table A.2: SPI Interface characteristics

INTERFACE DATA SHEET				
	I/F Designation:	**CAN interface**		
ID	**CAN Bus characteristics**		Ver	Iss
-1	Bus 1	compliant with ISO 11898–1[59] (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0 Supports time triggered CAN (TT-FDCAN) specified in ISO 11898–4[60]		
-2	Bus 2	compliant with ISO 11898–1[59] (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0		
-3	Receiver common mode input voltage	+/-12V		
-4	Bus fault protection	+/-58V		
-5	Max differential voltage between CANH and CANL	+/-45V		
-6	Bus termination	120 Ω at each end of the bus. Split termination is supported		

Table A.3: CAN Interface characteristics

INTERFACE DATA SHEET				
	I/F Designation:	**Antenna interface**		
ID	**RF characteristics**		Ver	Iss
-1	UHF Impedance	50 Ω		
-2	S-Band impedance	50 Ω		
Deployment control				
-3	Output type	Push-pull or Open-drain		
-4	Output voltage	Push-pull: 3.3V Open-drain: 5V		
-5	Output current	Max 18mA		
Deployment detection				
-6	Input type	Pull-Up, Pull-Down or Floating		
-7	Input voltage	Nominal 3.3V Tolerant 5V		
-8	High threshold	2V		
-9	Low threshold	0.8V		
-10	Pull-up/Pull-down resistor	40kΩ±10kΩ		

Table A.4: Antenna Interface characteristics

B. Modulation and Coding

B.1 Supported Modulation and Coding Schemes

Table B.1 provides the available modulation, framing and coding schemes as well as the symbol rates that are supported by the SatNOGS COMMS board. The board provides a set of schemes that are handled by the baseband core of the AT86RF215 IC and another utilizing the IQ interface of this IC and the onboard FPGA. The first set requires less power but exhibits several limitations (e.g. CC FEC available only for downlink, limited symbol rate configurations), whereas the later provides more flexibility and RF performance, at a cost of an increased power budget.

The achievable bitrate for every case depends on the FEC used and the bits per symbol of the corresponding modulation scheme. Specifically for the DSSS case, the achievable bitrate depends on the spreading factor. For more information of the available spreading factors refer to [1].

B.2 Performance

The majority of the decoding processing blocks operate in a per-frame basis, therefore performance experiments are based on the FER to estimate the achievable BER using the Equation B.1.

$$FER = 1 - (1 - BER)^N, N = \text{frame length in bits} \tag{B.1}$$

All of the BER evaluation experiments are using all of the DSP processing blocks, including clock recovery, synchronization and equalization. In addition, the input filtering is more relaxed regarding the occupied bandwidth, to allow for small offsets from the center frequency due to Doppler or other signal impairments. The resulting BER is related to the performance of the algorithms of these DSP tasks and how they perform under different SNR environments. For high SNR environments the implementation loss is up to 3dB with respect of the theoretical BER. However, the performance at low SNR scenarios is limited by the performance of the aforementioned processing blocks and may result to a larger deviation from the theoretical expected performance. While there is not a formal definition, for the evaluation of the transceiver a high SNR is

Baseband						
Modulation	**Framing**	**Line Coding**	**Whitening**	**Symbol Rate (ksps)**	**FEC**	**Modulation index**
FSK/MSK	IEEE 802.15.4	-	Off IEEE 802.15.4	50, 100, 150, 200, 300, 400	Off RS (223,255) CC R=1/2 CC R=1/2 + RS	0.375, 0.5, 0.75, 1, 1.25, 1.5, 1.75, 2
	CCSDS	Off NRZ-M	Off CCSDS	50, 100, 150, 200, 300, 400	Off RS (223,255) CC R=1/2 CC R=1/2 + RS	0.375, 0.5, 0.75, 1, 1.25, 1.5, 1.75, 2
O-QPSK DSSS	IEEE 802.15.4	-	Off IEEE 802.15.4	100, 200, 1000, 2000	-	-
IQ Mode (DSP on FPGA)						
FSK/MSK	IEEE 802.15.4 CCSDS	Off NRZ-M SP-L	Off IEEE 802.15.4 CCSDS	4.8, 9.6, 19.2, 20, 40, 50, 80,100, 125, 150, 200, 250, 300, 400, 500, 600, 800, 1000, 1200, 1400, 1800, 2000	Off RS (223, 255) CC R=1/2 CC R=1/2 + RS	0.375, 0.5, 0.75, 1, 1.25, 1.5, 1.75, 2
BPSK	IEEE 802.15.4 CCSDS	Off NRZ-M SP-L	Off IEEE 802.15.4 CCSDS	4.8, 9.6, 19.2, 20, 40, 50, 80,100, 125, 150, 200, 250, 300, 400, 500, 600, 800, 1000, 1200, 1400, 1800, 2000	Off RS (223, 255) CC R=1/2 CC R=1/2 + RS	π, $\frac{\pi}{2}$
QPSK	IEEE 802.15.4 CCSDS	Off NRZ-M SP-L	Off IEEE 802.15.4 CCSDS	4.8, 9.6, 19.2, 20, 40, 50, 80,100, 125, 150, 200, 250, 300, 400, 500, 600, 800, 1000, 1200, 1400, 1800, 2000	Off RS (223, 255) CC R=1/2 CC R=1/2 + RS	-

Table B.1: Available modulation, framing and coding schemes

assumed the SNR that contributes to a BER of 10^-5 or less, whereas a low SNR is 3-dB less than that.

Figure B.1 and B.2 depict the BER performance of the receivers for 2-FSK and BPSK respectively for different $Eb/N0$ values. The framing used for these experiments is the IEEE 802.15.4, with 12 bytes preamble and a 3 byte SFD. The frame is 64 bytes long and the data are scrambled using the CCSDS scrambler.

Figure B.3 and B.4 present the effect of the frequency offset at the perceived performance of the system for FSK and BPSK respectively. As expected, the FSK is more resilient to frequency offset due to the easier blind frequency offset compensation that is performed in DSP.

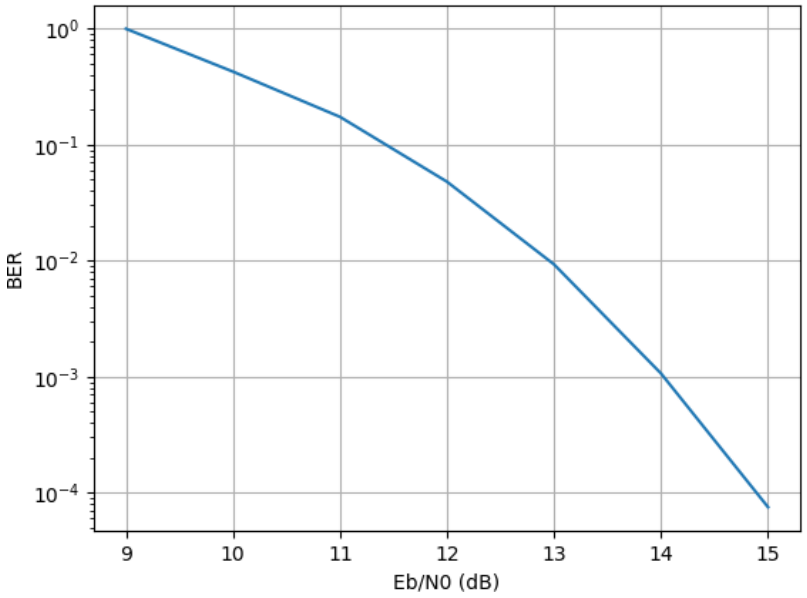

Figure B.1: Uncoded 2-FSK h=0.5 BER

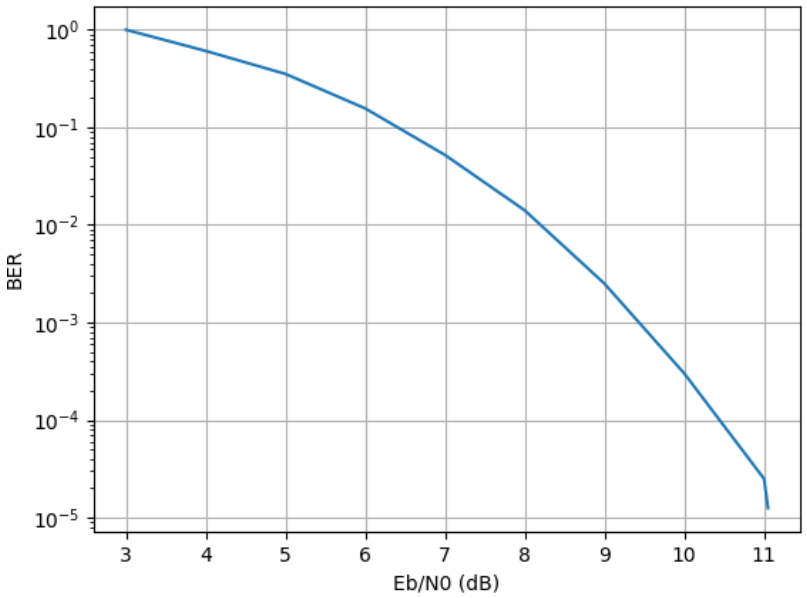

Figure B.2: Uncoded BPSK BER

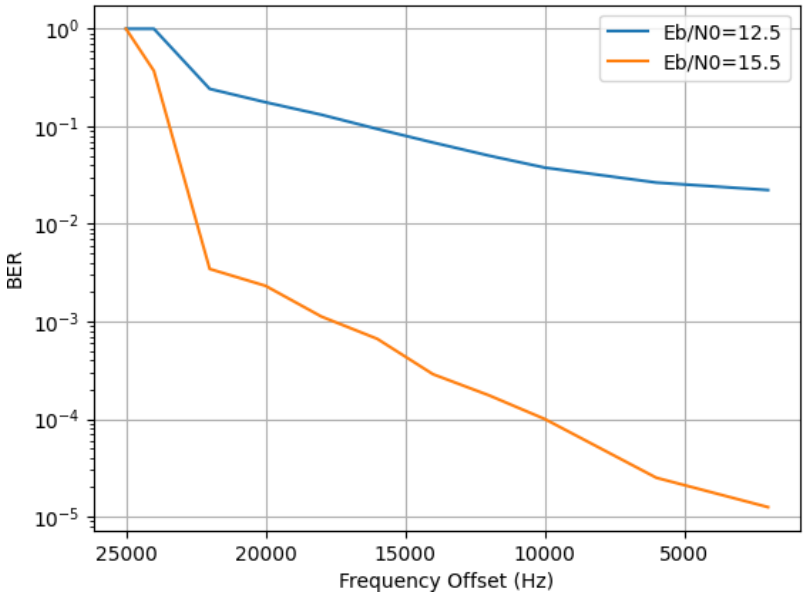

Figure B.3: BER vs Frequency offset for 2-FSK h=0.5

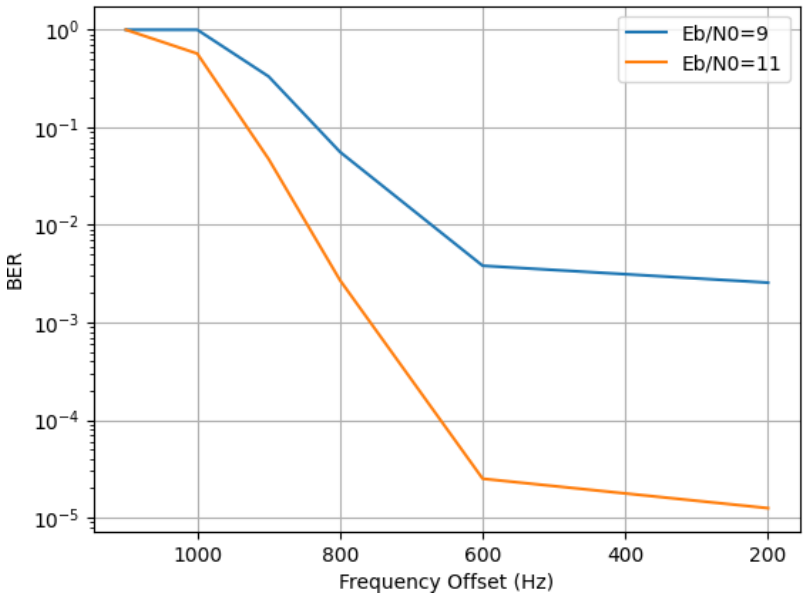

Figure B.4: BER vs Frequency offset for BPSK

C. Link Budget

Table C.1: Link Budget Rationale

Transmitter - Parameters	**Rationale**
Transmitter Frequency (MHz)	
Transmitter Power (dBm)	Assumption
Transmitter Power (dBW)	Transmitter Power (dBm)-30
Antenna circuit loss(RFDN) (dB)	SatNOGS UHF and S-Band GS
Antenna gain (dBi)	
Δ3dB antenna (deg)	
Pointing accuracy (deg)	
EIRP(dBW)	Transmitter Power (dBW)+RFDN (dB)+Antenna gain (dBi)
EIRP(dBm)	Transmitter Power (dBm)+RFDN (dB)+Antenna gain (dBi)
Path – Parameters	
Elevation angle (deg)	gr-leo
Altitude (km)	gr-leo
Slant Range (km)	gr-leo
Free Space Loss (dB)	gr-leo
Atmospheric/Ionospheric Loss (dB)	gr-leo
Rainfall Loss (dB)	gr-leo
Total Path Loss (dB)	Sum of Path losses
Receiver – Parameters	
Polarization loss (dB)	IARU Link Budget
Pointing loss (dB)	IARU Link Budget
Δ3dB antenna (deg)	
Pointing accuracy (deg)	Assumption
Antenna circuit loss(RFDN) (dB)	
Antenna gain (dBi)	
Total gain antenna(dB)	Polarization loss (dB)+Pointing Loss(dB)+RFDN(dB)+Antenna Gain(dBi)
Antenna Noise Temp (k)	
Received Signal (dBm)	EIRP(dBm) + Total Path Loss (dB) + Total Antenna Gain(dB)
Receiver – Performance	
Front-End NF(dB)	
Front-End Noise Temp (K) at 290K	
Tsys(K)	Antenna Noise Temp (K)+Front-End Noise Temp (K)
Tsys(dBK)	10*LOG10(Tsys)
G/T(dB/K)	Tsys(dBK)–Total Antenna Gain(dB)
Noise Floor (dBm/Hz)	10*LOG10(k*1000*Tsys(K))
Symbol rate (samples/s)	
Channel symbol rate (dBHz)	10*LOG10(Symbol Rate(samples/s))
Implementation Loss (dB)	Assumption
Received Es/N0(dB)	EIRP(dBW)+Total Path Loss(dB)+G/T(dB/K)+Impl. Loss(dB) -(k(dBW/(KHz))+Symbol Rate(dBHz))
RF Carrier Modulation, Type	
RF Carrier Modulation, Format	
User Bit Rate, b/s	The bitrate that the user of the system will observe
Bit Error Rate	ECSS-E-HB-50A
Data Coding, Type	
Required Bandwidth (Hz)	
Symbols M-arity	The number of different symbols supported by the modulation
Coding rate	
Received Eb/N0(dB)	Es/N0(Rx) -10*LOG10(LOG2(M-arity))-10*LOG10(Coding Rate)
Required Eb/N0(dB)	CCSDS 130.1-G-3
Margin (dB)	Received Eb/N0(dB)–Required Eb/N0(dB), >3dB according to ECSS-E-ST-50-05C [29]
Power Flux Density Budget	
PFD—Received (dB(W/m^2)) in 4kHz At Required Bandwidth	EIRP(dBW) -20*LOG10(Slant Range(m)) -10*LOG10(Required Bandwidth(Hz)/4000)-10*LOG10(4*π)
PFD – Limit (dB(W/m^2)) in 4kHz	For UHF is used the WRC-19 Final Acts [61], addition in 5.260A
PFD – Margin (dB)	PFD Limit–PFD Received

Table C.2: S-Band Uplink

Transmitter - Parameters				
Transmitter Frequency (MHz)	2025-2110	2025-2110	2025-2110	2025-2110
Transmitter Power (dBm)	40.00	40.00	40.00	40.00
Transmitter Power (dBW)	10.00	10.00	10.00	10.00
Antenna circuit loss(RFDN) (dB)	-1.00	-1.00	-1.00	-1.00
Antenna gain (dBi)	32.00	32.00	32.00	32.00
Δ3dB antenna (deg)	5.00	5.00	5.00	5.00
Pointing accuracy (deg)	1.00	1.00	1.00	1.00
EIRP(dBW)	41.00	41.00	41.00	41.00
EIRP(dBm)	71.00	71.00	71.00	71.00
Path – Parameters				
Elevation angle (deg)	5.22	25.42	5.23	25.15
Altitude (km)	400.00	400.00	600.00	600.00
Slant Range (km)	1842.05	868.61	2192.92	1121.96
Free Space Loss (dB)	-164.99	-158.46	-166.51	-160.68
Atmospheric/Ionospheric Loss (dB)	-2.04	-0.45	-2.04	-0.46
Rainfall Loss (dB)	-0.002	-0.002	-0.002	-0.002
Total Path Loss (dB)	-167.04	-158.91	-168.54	-161.15
Receiver – Parameters				
Polarization loss (dB)	-0.30	-0.30	-0.30	-0.30
Pointing loss (dB)	-1.50	-1.50	-1.50	-1.50
Δ3dB antenna (deg)	80.00	80.00	80.00	80.00
Pointing accuracy (deg)	1.00	1.00	1.00	1.00
Antenna circuit loss(RFDN) (dB)	-1.00	-1.00	-1.00	-1.00
Antenna gain (dBi)	7.00	7.00	7.00	7.00
Total Antenna Gain(dB)	4.20	4.20	4.20	4.20
Antenna Noise Temp (K)	290.00	290.00	290.00	290.00
Received Signal (dBm)	-91.84	-83.71	-93.34	-85.95
Receiver – Performance				
Front-End NF(dB)	1.30	1.30	1.30	1.30
Front-End Noise Temp (K) at 290K	101.20	101.20	101.20	101.20
Tsys(K)	391.20	391.20	391.20	391.20
Tsys(dBK)	25.92	25.92	25.92	25.92
G/T(dB/K)	-21.72	-21.72	-21.72	-21.72
Noise Floor (dBm/Hz)	-184.46	-184.46	-184.46	-184.46
Symbol rate (samples/s)	2000000.00	2000000.00	2000000.00	2000000.00
Channel symbol rate (dBHz)	63.01	63.01	63.01	63.01
Implementation Loss (dB)	-3.00	-3.00	-3.00	-3.00
Received Es/N0(dB)	14.83	22.95	13.32	20.72
RF Carrier Modulation, Type	BPSK	BPSK	BPSK	BPSK
RF Carrier Modulation, Format	SP-L	SP-L	SP-L	SP-L
User Bit Rate, b/s	430502	430502	430502	430502
Bit Error Rate	10^{-5}	10^{-5}	10^{-5}	10^{-5}
Data Coding, Type	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)
Required Bandwidth (Hz)	2700000.00	2700000.00	2700000.00	2700000.00
Symbols M-arity	2.00	2.00	2.00	2.00
Coding rate	0.43	0.43	0.43	0.43
Received Eb/N0(dB)	18.49	26.62	16.98	24.38
Required Eb/N0(dB)	2.30	2.30	2.30	2.30
Margin (dB)	16.19	24.32	14.68	22.08

Table C.3: S-Band Downlink

Transmitter - Parameters				
Transmitter Frequency (MHz)	2200-2290	2200-2290	2200-2290	2200-2290
Transmitter Power (dBm)	31.30	31.30	31.30	31.30
Transmitter Power (dBW)	1.30	1.30	1.30	1.30
Antenna circuit loss(RFDN) (dB)	-1.00	-1.00	-1.00	-1.00
Antenna gain (dBi)	7.00	7.00	7.00	7.00
Δ3dB antenna (deg)	80.00	80.00	80.00	80.00
Pointing accuracy (deg)	1.00	1.00	1.00	1.00
EIRP(dBW)	7.30	7.30	7.30	7.30
EIRP(dBm)	37.30	37.30	37.30	37.30
Path – Parameters				
Elevation angle (deg)	5.22	37.20	5.23	25.15
Altitude (km)	400.00	400.00	600.00	600.00
Slant Range (km)	1842.05	657.51	2192.92	1121.96
Free Space Loss (dB)	-164.99	-156.04	-166.51	-160.68
Atmospheric/Ionospheric Loss (dB)	-2.04	-0.32	-2.04	-0.46
Rainfall Loss (dB)	-0.002	-0.003	-0.0021	-0.0021
Total Path Loss (dB)	-167.04	-156.37	-168.55	-161.14
Receiver – Parameters				
Polarization loss (dB)	-0.30	-0.30	-0.30	-0.30
Pointing loss (dB)	-1.50	-1.50	-1.50	-1.50
Δ3dB antenna (deg)	5.00	5.00	5.00	5.00
Pointing accuracy (deg)	1.00	1.00	1.00	1.00
Antenna circuit loss(RFDN) (dB)	-1.00	-1.00	-1.00	-1.00
Antenna gain (dBi)	32.00	32.00	32.00	32.00
Total gain antenna(dB)	29.20	29.20	29.20	29.20
Antenna Noise Temp (K)	750.00	300.00	750.00	400.00
Received Signal (dBm)	-100.54	-89.87	-102.05	-94.64
Receiver – Performance				
Front-End NF(dB)	1.30	1.30	1.30	1.30
Front-End Noise Temp (K) at 290K	101.20	101.20	101.20	101.20
Tsys(K)	851.20	401.20	851.20	501.20
Tsys(dBK)	29.30	26.03	29.30	27.00
G/T(dB/K)	-0.10	3.17	-0.10	2.20
Noise Floor (dBm/Hz)	-183.93	-184.45	-183.93	-184.29
Symbol rate (samples/s)	2000000.00	2000000.00	2000000.00	2000000.00
Channel symbol rate (dBHz)	63.01	63.01	63.01	63.01
Implementation Loss (dB)	-3.00	-3.00	-3.00	-3.00
Received Es/N0(dB)	2.75	16.69	1.24	10.95
RF Carrier Modulation, Type	BPSK	BPSK	BPSK	BPSK
RF Carrier Modulation, Format	NRZ-M	NRZ-M	NRZ-M	NRZ-M
User Bit Rate, b/s	860000	860000	860000	860000
Bit Error Rate	10^{-5}	10^{-5}	10^{-5}	10^{-5}
Data Coding, Type	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)
Required Bandwidth (Hz)	2700000.00	2700000.00	2700000.00	2700000.00
Symbols M-arity	2.00	2.00	2.00	2.00
Coding rate	0.43	0.43	0.43	0.43
Received Eb/N0(dB)	6.42	20.35	4.90	14.61
Required Eb/N0(dB)	2.30	2.30	2.30	2.30
Margin (dB)	4.12	18.05	2.60	12.31
Power Flux Density Budget				
PFD – Received (dB(W/m^2)) in 4kHz At Required Bandwidth	-157.29	-148.34	-158.80	-152.98
PFD – Limit (dB(W/m^2)) in 4kHz	-154.00	-144.00	-154.00	-144.00
PFD – Margin (dB)	3.29	4.34	4.80	8.98

Table C.4: UHF Uplink

Transmitter - Parameters				
Transmitter Frequency (MHz)	400-500	400-500	400-500	400-500
Transmitter Power (dBm)	47.00	47.00	47.00	47.00
Transmitter Power (dBW)	17.00	17.00	17.00	17.00
Antenna circuit loss(RFDN) (dB)	-1.00	-1.00	-1.00	-1.00
Antenna gain (dBi)	16.00	16.00	16.00	16.00
Δ3dB antenna (deg)	30.00	30.00	30.00	30.00
Pointing accuracy (deg)	1.00	1.00	1.00	1.00
EIRP(dBW)	32.00	32.00	32.00	32.00
EIRP(dBm)	62.00	62.00	62.00	62.00
Path – Parameters				
Elevation angle (deg)	5.22	31.38	5.23	25.03
Altitude (km)	400.00	400.00	600.00	600.00
Slant Range (km)	1842.05	745.34	2192.92	1125.25
Free Space Loss (dB)	-150.43	-142.57	-151.94	-146.14
Atmospheric/Ionospheric Loss (dB)	-2.06	-0.38	-2.06	-0.46
Rainfall Loss (dB)	-0.003	-0.001	-0.003	-0.001
Total Path Loss (dB)	-152.49	-142.95	-154.00	-146.61
Receiver – Parameters				
Polarization loss (dB)	-0.30	-0.30	-0.30	-0.30
Pointing loss (dB)	0.00	0.00	0.00	0.00
Δ3dB antenna (deg)	Close to omni	Close to omni	Close to omni	Close to omni
Pointing accuracy (deg)	1.00	1.00	1.00	1.00
Antenna circuit loss(RFDN) (dB)	-1.00	-1.00	-1.00	-1.00
Antenna gain (dBi)	1.50	1.50	1.50	1.50
Total gain antenna(dB)	0.20	0.20	0.20	0.20
Antenna Noise Temp (k)	290.00	290.00	290.00	290.00
Received Signal (dBm)	-90.29	-80.75	-91.80	-84.41
Receiver – Performance				
Front-End NF(dB)	1.70	1.70	1.70	1.70
Front-End Noise Temp (K) at 290K	138.94	138.94	138.94	138.94
Tsys(K)	428.94	428.94	428.94	428.94
Tsys(dBK)	26.32	26.32	26.32	26.32
G/T(dB/K)	-26.12	-26.12	-26.12	-26.12
Noise Floor (dBm/Hz)	-184.40	-184.40	-184.40	-184.40
Symbol rate (samples/s)	2000000.00	2000000.00	2000000.00	2000000.00
Channel symbol rate (dBHz)	63.01	63.01	63.01	63.01
Implementation Loss (dB)	-3.00	-3.00	-3.00	-3.00
Received Es/N0(dB)	15.98	25.52	14.47	21.86
RF Carrier Modulation, Type	BPSK	BPSK	BPSK	BPSK
RF Carrier Modulation, Format	SP-L	SP-L	SP-L	SP-L
User Bit Rate, b/s	430502	430502	430502	430502
Bit Error Rate	10^{-5}	10^{-5}	10^{-5}	10^{-5}
Data Coding, Type	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)
Required Bandwidth (Hz)	2700000.00	2700000.00	2700000.00	2700000.00
Symbols M-arity	2.00	2.00	2.00	2.00
Coding rate	0.43	0.43	0.43	0.43
Received Eb/N0(dB)	19.64	29.18	18.13	25.52
Required Eb/N0(dB)	2.30	2.30	2.30	2.30
Margin (dB)	17.34	26.88	15.83	23.22

Table C.5: UHF Downlink

Transmitter - Parameters				
Transmitter Frequency (MHz)	400-500	400-500	400-500	400-500
Transmitter Power (dBm)	32.30	32.30	32.30	32.30
Transmitter Power (dBW)	2.30	2.30	2.30	2.30
Antenna circuit loss(RFDN) (dB)	-1.00	-1.00	-1.00	-1.00
Antenna gain (dBi)	1.50	1.50	1.50	1.50
Δ3dB antenna (deg)	Close to omni	Close to omni	Close to omni	Close to omni
Pointing accuracy (deg)	1.00	1.00	1.00	1.00
EIRP(dBW)	2.80	2.80	2.80	2.80
EIRP(dBm)	32.80	32.80	32.80	32.80
Path – Parameters				
Elevation angle (deg)	5.00	31.38	5.23	25.03
Altitude (km)	400.00	400.00	600.00	600.00
Slant Range (km)	1858.55	745.34	2192.92	1125.25
Free Space Loss (dB)	-153.00	-142.57	-151.94	-146.14
Atmospheric/Ionospheric Loss (dB)	-0.04	-0.38	-2.06	-0.46
Rainfall Loss (dB)	0.00	-0.0012	-0.0033	-0.0012
Total Path Loss (dB)	-153.04	-142.95	-154.00	-146.61
Receiver – Parameters				
Polarization loss (dB)	-0.30	-0.30	-0.30	-0.30
Pointing loss (dB)	0.00	0.00	0.00	0.00
Δ3dB antenna (deg)	30.00	30.00	30.00	30.00
Pointing accuracy (deg)	1.00	1.00	1.00	1.00
Antenna circuit loss(RFDN) (dB)	-1.00	-1.00	-1.00	-1.00
Antenna gain (dBi)	16.00	16.00	16.00	16.00
Total gain antenna(dB)	14.70	14.70	14.70	14.70
Antenna Noise Temp (k)	3000.00	350.00	3000.00	350.00
Received Signal (dBm)	-105.54	-95.45	-106.50	-99.11
Receiver – Performance				
Front-End NF(dB)	1.70	1.70	1.70	1.70
Front-End Noise Temp (K) at 290K	138.94	138.94	138.94	138.94
Tsys(K)	3138.94	488.94	3138.94	488.94
Tsys(dBK)	34.97	26.89	34.97	26.89
G/T(dB/K)	-20.27	-12.19	-20.27	-12.19
Noise Floor (dBm/Hz)	-183.16	-184.30	-183.16	-184.30
Symbol rate (samples/s)	2000000.00	2000000.00	2000000.00	2000000.00
Channel symbol rate (dBHz)	63.01	63.01	63.01	63.01
Implementation Loss (dB)	-3.00	-3.00	-3.00	-3.00
Received Es/N0(dB)	-7.92	10.25	-8.88	6.59
RF Carrier Modulation, Type	BPSK	BPSK	BPSK	BPSK
RF Carrier Modulation, Format	NRZ-M	NRZ-M	NRZ-M	NRZ-M
User Bit Rate, b/s	861004	861004	861004	861004
Bit Error Rate	10^{-5}	10^{-5}	10^{-5}	10^{-5}
Data Coding, Type	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)	CC(7,1/2) /RS(255,223)
Required Bandwidth (Hz)	2700000.00	2700000.00	2700000.00	2700000.00
Symbols M-arity	2.00	2.00	2.00	2.00
Coding rate	0.43	0.43	0.43	0.43
Received Eb/N0(dB)	-4.26	13.91	-5.22	10.25
Required Eb/N0(dB)	2.30	2.30	2.30	2.30
Margin (dB)	-6.56	11.61	-7.52	7.95
Power Flux Density Budget				
PFD – Received (dB(W/m^2)) in 4kHz At Required Bandwidth	-161.87	-153.93	-163.30	-157.51
PFD – Limit (dB(W/m^2)) in 4kHz	-131.38	-123.44	-132.81	-127.02
PFD – Margin (dB)	30.49	30.49	30.49	30.49

D. RFFC5071 Evaluation

D.1 Conversion loss

According to data-sheet of RFFC5071 [14] the conversion loss or gain is -2dB with out including balun losses. From diagram in page 19 of datasheet the conversion gain is measured in evaluation board of RFFC5071, for constant $IF = 100MHz$ and variable RF and LO. For $VCC = 3.3V$ and $T = 27°C$ the conversion gain is -4dB to -5dB. In our development board of the RFFC5071 [62] for $LO = 200MHz$, $IF = 2250MHz$ and $RF = 2450MHz$ for various RF power inputs the conversion gain is 7.5dB to 10dB as it seems in table D.1. The difference of data-sheet and the development board is due to impedance matching.

IF (dBm)	RF (dBm)	G (dB)
-28.14	-20	-8.14
-48.4	-40	-8.41
-38	-30	-8
-90.2	-80	-10.2
-97.7	-90	-7.7

Table D.1: RFFC5071 Conversion Gain

D.2 Isolation and Local Oscillator Harmonics

The isolation between ports LO-RF and LO-IF are measured according to application note, Mini-Circuits AN-00–009 [63]. By setting the register BYPAS [64] of RFFC5071 to 1 the LO is appeared to the output of mixer-1 (IF-RX port). In the RF column in table D.2 is the LO leakage in RF port, in the IF column is the LO leakage in IF port. The LO frequency is 200MHz.

F (MHz)	LO (dBm)	RF (dBm)	IF (dBm)
200	-19.7	-83	-57
400	-23.14	-64	-19.6
600	-3.41	-82	-39.6
800	-31.3	-55.5	-29.1
1000	-12.7	-60.2	-46.8
1200	-36.5	-54.3	-30.5
1400	-12.4	-65.2	-61
1600	-52.6	-56.4	-39.8
1800	-16.3	-72	-63.2
2000	-52.5	-62.3	-50.1
2200	-22.66	-71	-75
2400	-49.5	-57.6	-58.6
2600	-23.5	-67	-61
2800	-51.2	-49	-54

Table D.2: LO leakage to RF and IF port, LO=200MHz

The measurements are done in same bandwidth 500kHz and noise floor is -90dBm. Then change the LO frequency to 400MHz, table D.3.

F (MHz)	LO (dBm)	RF (dBm)	IF (dBm)
400	-3.94	-74	-31.5
800	-29.3	-53.1	-24
1200	-6.7	-54.3	-44.8
1600	-40	-55.5	-34.4
2000	-14	-61.3	-60.8
2400	-44	-53.46	-52.4
2800	-16.1	-59.1	-56.1

Table D.3: LO leakage to RF and IF port, LO=400MHz

These measurements are done for mix current register is set to 1. From above measurements, it seems that the harmonics are spread out in all spectrum, that means the LO is a square wave signal. In the tableD.4 in calculated the conversion gain when

the tuned frequency in near a harmonic of LO=400MHz:

RF (MHz)	IF (MHz)	RF (dBm)	IF (dBm)	Conversion Gain (dB)
2400	2000	-5	-15.18	10.18
2410	2010	-5	-15.7	10.7
2420	2020	-5	-15.7	10.7
2430	2030	-5	-15.35	10.35
2440	2040	-5	-14.63	9.63
2450	2050	-5	-14.4	9.4
2460	2060	-5	-14.1	9.1
2470	2070	-5	-14.1	9.1
2480	2080	-5	-13.8	8.8
2490	2090	-5	-13.4	8.4
2500	2100	-5	-12.94	7.94
2510	2110	-5	-12.93	7.93
2520	2120	-5	-13.4	8.4
2530	2130	-5	-14.04	9.04
2540	2140	-5	-14.8	9.8
2550	2150	-5	-15.63	10.63

Table D.4: Conversion Gain, LO=400MHz

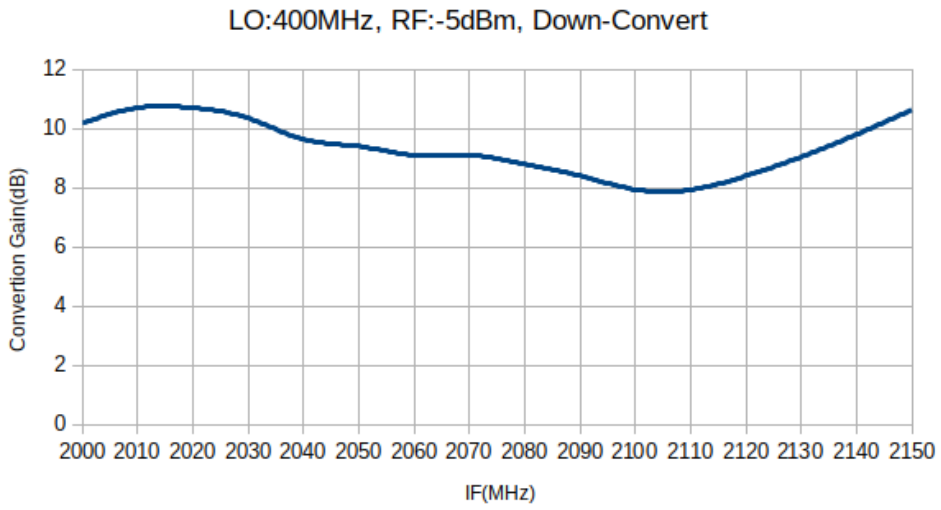

Figure D.1: Conversion Gain, LO=400MHz

It is necessary to avoid the operation near LO harmonics to have a better conversion gain.

D.3 P1dB, MDS, Linear Dynamic Range

To calculate the P1dB we follow the application note, Mini-Circuits AN-00–009 [63]. For RF 2450MHz and LO 200MHz and mix current register is set to 4, the input P1dB is 12dBm, figure D.2.

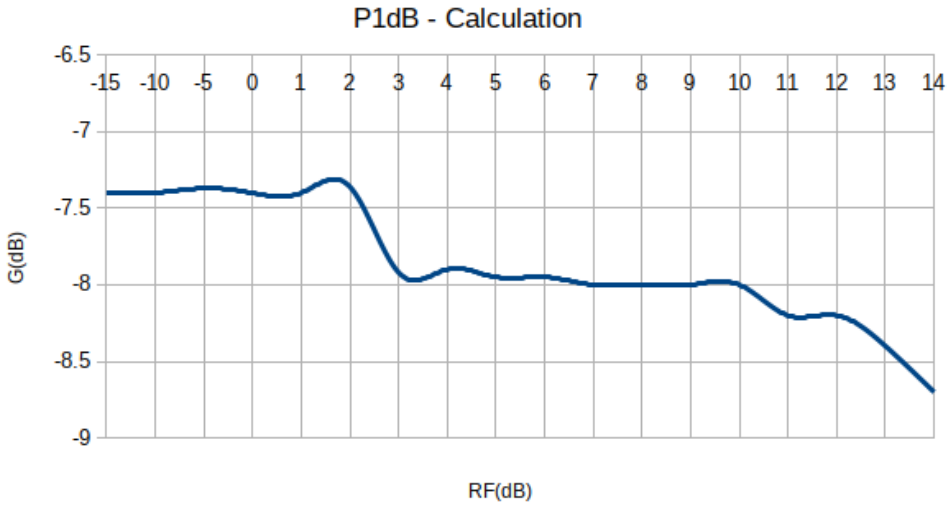

Figure D.2: Input P1dB, LO=200MHz, RF=2450MHz and mixer current register is set to 4

The MDS is measured with spectrum bandwidth of 5kHz, for RF signal of 2350MHz at -100dBm, LO frequency 200MHz and mix current register is set to 4, the IF signal is -92.3dBm at 2450MHz and noise floor is -108dBm. So the linear dynamic range is -96.9dB.

E. Failure Modes and Effects Analysis

Product: SatNOGS COMMS	**System:** SatNOGS COMMS transceiver	**Subsystem:** Power supply	**Equipment:** NA
Id. Number: 1	**Item/block:** Power supply MOSFET		
Function: Provide voltage regulation for the entire transceiver			
Failure mode: Power MOSFET latch-up			
Failure cause: Radiation environment			
Mission phase: In-orbit			
Failure effects: 1. **Local effects**: Voltage exceeds operational limits, high power consumption, possibility of fire, smoke and/or sparks 2. **End effects**: Communication loss with the transceiver (either from ground or other spacecraft subsystems), loss of the transfer vehicle			
Severity classification: Catastrophic. Failure propagation can lead to loss of the spacecraft and loss of life			
Failure detection method/Observable symptoms: High or zero power consumption, communication loss through the bus, temperature increase			
Compensating provisions: MOSFET latch recovery is carried out by power cycling affected DCDC converters and components via a hardware over voltage supervisor			
Recommendations: Use a radiation hardened MOSFET, transceiver should be powered off during launch operations and until the deployment from the mother-ship			
Remarks: The use of a radiation hardened MOSFET is prohibitive in terms of cost and real estate on the PCB. However, the transceiver tries to deal with the event of the MOSFET latch up, using a hardware overvoltage supervisor. When the supervisor identifies an overvoltage event, it cuts out the supply of the MOSFET allowing the system to recover			

Product: SatNOGS COMMS	**System:** SatNOGS COMMS transceiver	**Subsystem:** Power supply	**Equipment:** NA
Id. Number: 2	**Item/block:** PMIC		
Function: Voltage-current regulation and report			
Failure mode: The PMIC holds the voltage and current settings on memory registers. Bit flips on these registers can lead to output voltage that exceed the operational limits of various components			
Failure cause: Radiation environment			
Mission phase: In-orbit			
Failure effects: 1. **Local effects**: Over-voltage may destroy the FPGA and RAM modules. Some failed components may short circuit resulting to high power consumption and temperature increase. Possibility of fire, smoke and/or sparks 2. **End effects**: Communication loss with the FPGA, degraded RF modulation capabilities			
Severity classification: Catastrophic. Failure propagation can lead to loss of the spacecraft and loss of life			
Failure detection method/Observable symptoms: Power cycles triggered by the voltage protection supervisors			
Compensating provisions: The PMIC register file is periodically updated with the appropriate values by a software routine. The software responsible for the write operations at the register file, ensures also that the correct value was written, by doing also a read-back of the register values.			
Recommendations: Use a software-based routine that updates the register file of the PMIC in par with a hardware protection mechanism, transceiver should be powered off during launch operations and until the deployment from the mother-ship			
Remarks: In case of SEU, the reaction time of the software routine is orders of magnitude higher from the required, in order to avoid permanent damage on critical components due to overvoltage. Therefore, the power supply design protects these components using the hardware based supervisor. The software routine, ensures that the state of the PMIC will be restored in a nominal operating state, shortly after the bit flip at the PMIC register file.			

Product: SatNOGS COMMS	**System:** SatNOGS COMMS transceiver	**Subsystem:** Memory	**Equipment:** NA
Id. Number: 3	**Item/block:** MCU and FPGA RAM memory		
Function: Hold software state			
Failure mode: SEU may lead to bit flips resulting to erroneous software state either on the MCU and/or the FPGA			
Failure cause: Radiation environment			
Mission phase: In-orbit			
Failure effects: 1. **Local effects**: Erroneous operation states, software halt 2. **End effects**: Temporary loss of communication (either from ground or other spacecraft subsystems)			
Severity classification: Minor. Temporary mission degradation			
Failure detection method/Observable symptoms: Unpredicted system resets, watchdog system resets, hardware error detection mechanisms triggering ECC error events			
Compensating provisions: The STM32F743 [2] MCU has integrated ECC capabilities on all the available memory regions (RAM, cache). The hardware raises a dedicated interrupt in case an error is detected. The ZYNQ-7020 supports also ECC and notifications in case of memory errors. In the event of a memory error the system resets.			
Recommendations: Use software or hardware based ECC where applicable, integrate an independent hardware watchdog			
Remarks: Critical information can be protected using software techniques like higher order ECC (e.g Reed Solomon (223,255)) and/or TMR			

Product: SatNOGS COMMS	**System:** SatNOGS COMMS transceiver	**Subsystem:** Memory	**Equipment:** NA
Id. Number: 4	**Item/block:** Non-volatile memory		
Function: Retain the MCU and FPGA firmwares as well as information that should be persistent across system resets			
Failure mode: SEU may lead to bit flips in the non-volatile memory resulting to erroneous software state either on the MCU and/or the FPGA			
Failure cause: Radiation environment			
Mission phase: In-orbit			
Failure effects: 1. **Local effects**: Unbootable MCU firmware, erroneous or abnormal operation 2. **End effects**: Temporary or permanent loss of communication (either from ground or other spacecraft subsystems)			
Severity classification: Critical. Loss of mission			
Failure detection method/Observable symptoms: Unpredicted system resets, watchdog system resets, hardware error detection mechanisms triggering ECC error events			
Compensating provisions: The STM32F743 [2] MCU has integrated ECC capabilities on the available flash memory. In addition, an external flash memory holds multiple copies of the MCU and FPGA firmwares. Their integrity is ensured by two different hash digests.			
Recommendations: Use also TMR on the MCU and FPGA firmwares			
Remarks: Even if TMR is used to protect the firmware integrity, the bootloader firmware cannot be protected by software means. Therefore, is essential that the bootloader firmware is stored in the ECC capable flash memory bank of the STM32F743 [2] MCU. The bootloader can apply TMR techniques and load the main MCU firmware			

Product: SatNOGS COMMS	**System:** SatNOGS COMMS transceiver	**Subsystem:** Peripheral ICs	**Equipment:** NA
Id. Number: 5	**Item/block:** Register file of peripheral ICs		
Function: IC configuration and operation			
Failure mode: During write operations strong EMI on the communication bus (I2C, SPI) may cause erroneous information to be written. This can also happen due to MCU preemption, when a higher priority routine may interrupt and stop a communication transaction with an IC			
Failure cause: EMI, preemption			
Mission phase: In-orbit			
Failure effects: 1. **Local effects**: Erroneous or abnormal operation 2. **End effects**: Temporary loss of communication (either from ground or other spacecraft subsystems)			
Severity classification: Minor. Temporary mission degradation			
Failure detection method/Observable symptoms: Unpredicted system resets, watchdog system resets, abnormal telemetry values			
Compensating provisions: The SatNOGS COMMS transceiver incorporates a fault tolerant write & read-back technique. Every write on a peripheral IC register, is followed by a read-back to ensure that the correct information was written at the IC			
Recommendations: Use decoupling capacitors and proper shielding, reduce the communication speed with the MCU and the peripheral ICs			
Remarks: The compensating provisions can detect errors during a transaction with the IC. An error to the register file at runtime, (e.g due to SEU) cannot be detected by this mechanism			

F. Mass Budget

#	Component	Material	Mass (grams)
1	PCB	FR4 and copper	31.1
2	Passive Components	NA	7.1
3	ICs	NA	11.9
4	Connector	NA	6.0
5	Shield	Al 7075	41.2
6	Screws	A4 Stainless Steel	4.1
		TOTAL	101.4

Table F.1: Mass Budget Table

G. Worst Case Analysis for tolerances of sensitive circuits

G.1 Low Pass Filter

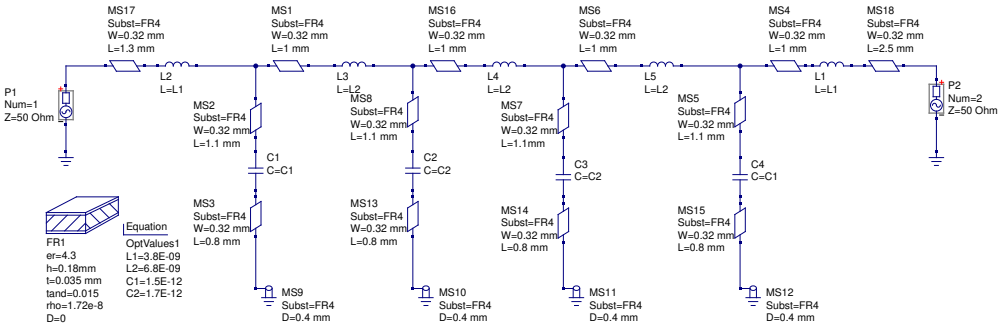

Figure G.1: S-Band Low Pass Filter

Manufacturer	Part Number	Value	Tolerance
Johanson Technology	201R07S1R5AV4T	1.5pF	0.05pF
Murata Electronics	LQG15WZ3N8B02D	3.8nH	0.1nH
TDK	MHQ1005P6N8GT000	6.8nH	0.136nH
Johanson Technology	500R07S1R7AV4T	1.7pF	0.05 pF

Table G.1: Low Pass Filter Passive Components

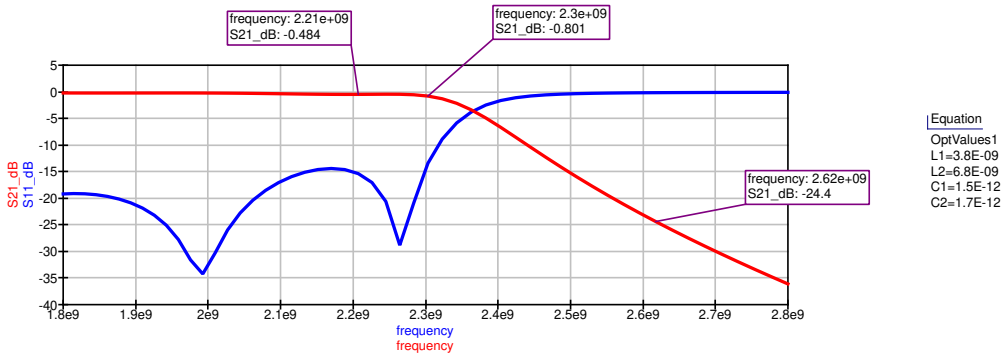

Figure G.2: Worst Case Analysis Case 0

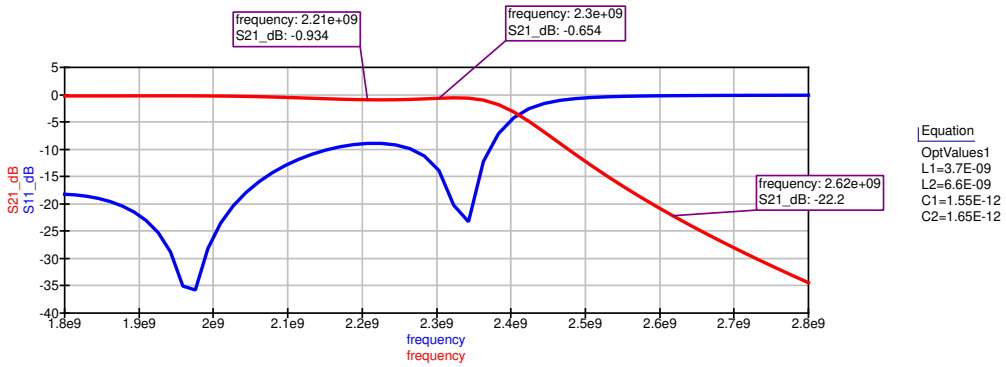

Figure G.3: Worst Case Analysis Case 1

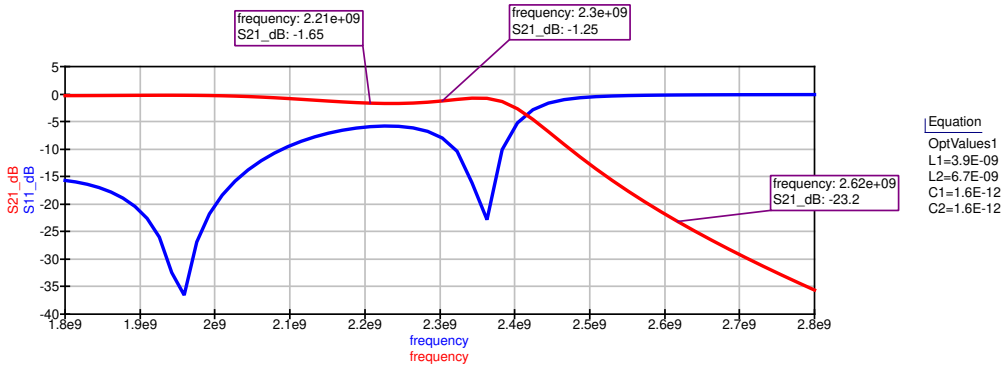

Figure G.4: Worst Case Analysis Case 2

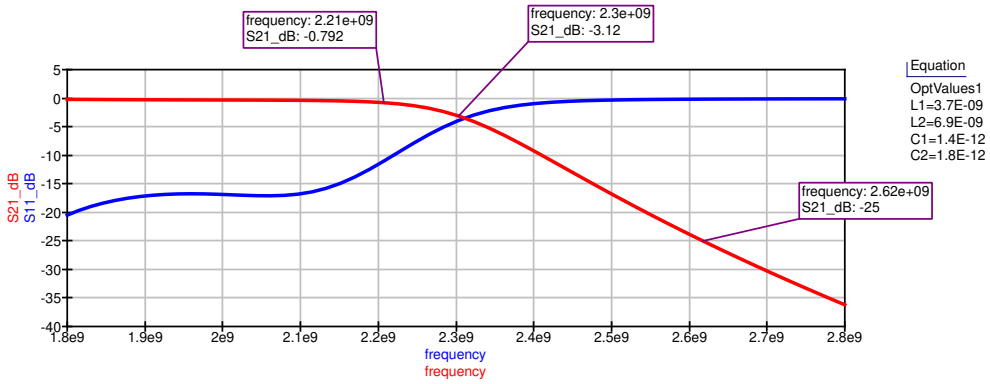

Figure G.5: Worst Case Analysis Case 3

G.2 UHF PA Matching Network

Manufacturer	Part Number	Value	Tolerance
Murata Electronics	GJM1555C1H2R0WB01D	2pF	0.05pF
Murata Electronics	LQG15WZ3N2B02D	3.2nH	0.1nH
TDK	MHQ1005P68NGTD25	68nH	1.36nH
AVX	04025U240FAT2A	24pF	0.24pF
AVX	04025A620FAT2A	62pF	0.62pF
TDK	MHQ1005P8N2GT000	8.2nH	0.164nH
Murata Electronics	GJM1555C1H3R3WB01D	3.3pF	0.05pF
ABRACON	AISC-0402-47NG-T	47nH	0.94nH

Table G.2: UHF PA Matching Network Passive Components

In matching network the L-match passive components play an important role instead compere to L-C in series. For that reason in worst case analysis the L-C in series components are constant. In figures G.7, G.8 are shown the results of analysis.

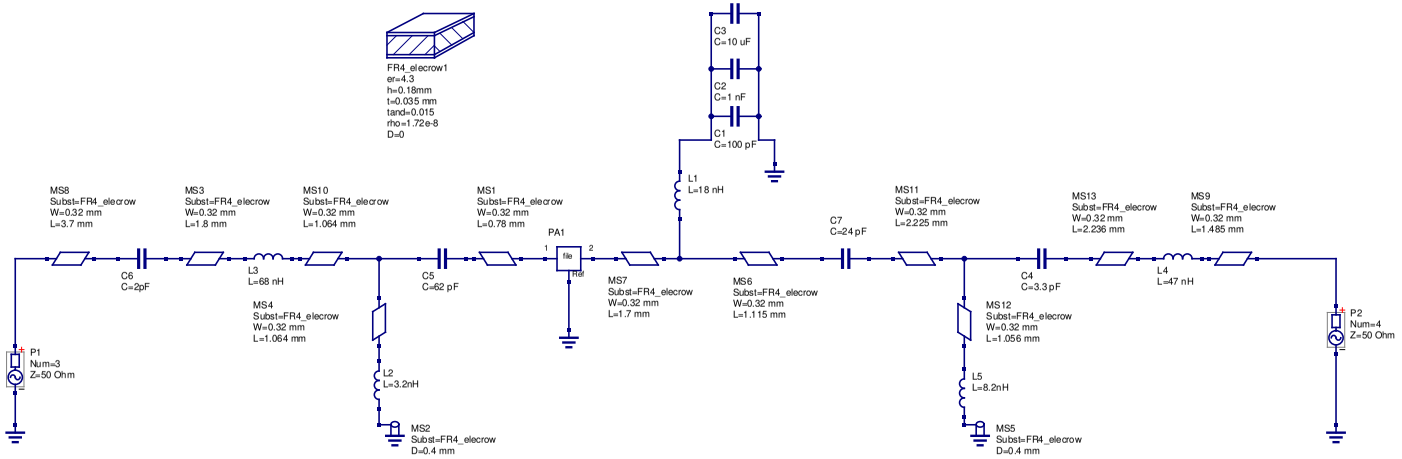

Figure G.6: UHF PA Matching Network

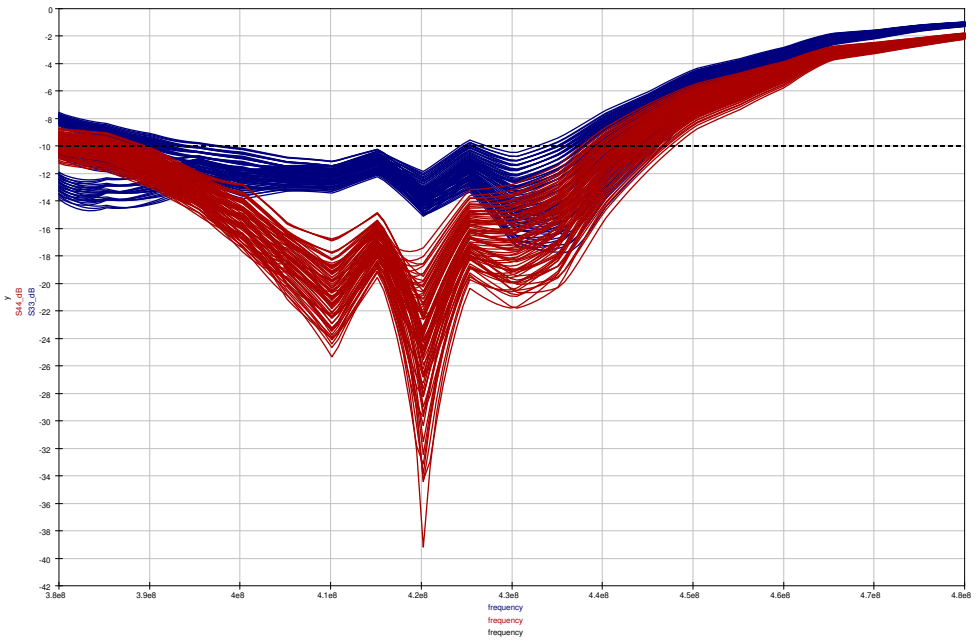

Figure G.7: UHF PA return loss in input and output

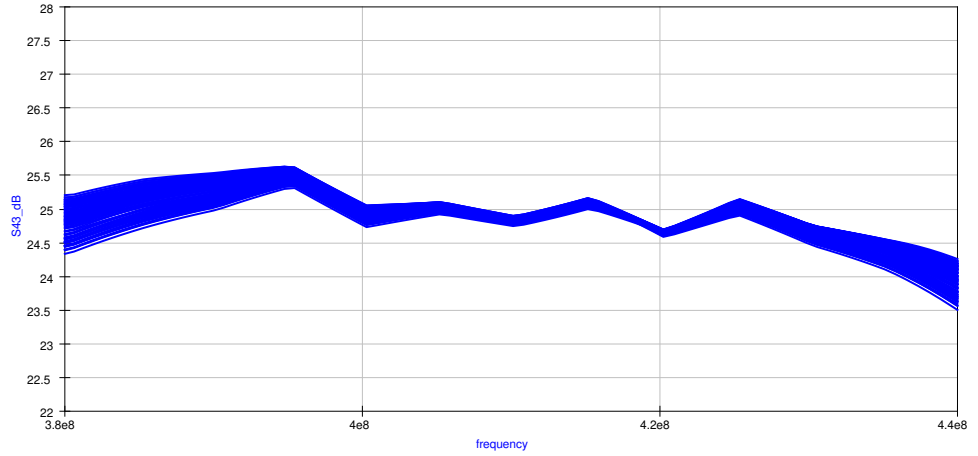

Figure G.8: HF PA gain

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