Design and Development Plan

SatNOGS COMMS

Libre Space Foundation

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1. Introduction

1.1 Purpose and Scope

This document describes design and development stages, activities and tasks of 'SatNOGS-COMMS'. It also include an update risk assessment of the design and development activities.

1.2 Acronyms

FPGA Field Programmable Gate Array

2. Design and Development

The development process is conducted in two parallel workgroups, one working on the space and the other working on the ground segment. Although there are no blocking dependencies between the groups, at least in early development phases, the working groups are in close collaboration through frequent common meetings and progress reports to ensure interoperability of the two segments and the testing campaign.

2.1 COMMS transceiver

For the COMMS subsystem, the hardware development is started by implementing a basic subset of the target functionality, so that software engineers can immediately start working on it. This breadboard model will accommodate the MCU, the FPGA and the RF IC. Debugging probes will also be available for easy access of critical signal paths. At this stage signal reception or transmission will be performed using only the capabilities of the RF IC. To keep the design complexity low, no external PAs or LNAs will be available, so testing will be performed in a controlled environment using a cabling and attenuator setup. GNU Radio based modulators/demodulators and SDR hardware devices will be used to test basic connectivity with the COMMS. Development on this board will provide feedback to the hardware design engineers and spot possible issues early in the development phase and improve them at the next iterations. As the software for the COMMS subsystem evolves, the hardware design will simulate the RF characteristics of the COMMS using the Qucs open source circuit simulator. At the time the COMMS subsystem becomes mature enough, a second design phase will start extending its capabilities with PAs and LNAs for the supported frequency bands. This is expected to be accomplished with several iterations allowing to an agile development and adaptation to the proposed requirements. With the appropriate LNAs and PAs attached on the subsystem, series of simulations will be conducted to identify if the performance of the board meets the requirements. The simulation will be done using the gr-leo GNU Radio simulator which will introduce the LEO channel impairments (noise, variable attenuation, doppler shift).

2.2 Ground Segment

For the ground segment, development of the new socket-based control and data interfaces will start on SatNOGS Radio in parallel with development on

SatNOGS Network to support handover, proxying and uplink scheduling. Once the new SatNOGS Radio interfaces stabilize, SatNOGS client development will begin in order to support these interfaces. Functional and integration testing will take place to ensure compatibility of new features between subcomponents. Using a test-driven development process, implementation of automated test cases can start in parallel or preferably before development starts. Development of ground segment will follow Agile principles, using an iterative approach to eventually satisfy all the specified requirements.

2.3 Verification

After completion of at least one iteration which implements a functional interface, integration testing will take place in order to provide fast feedback and detection of possible errors. Continuous Integration and Automated Testing will be used to reduce the time and effort for running these tests.

3. Updated Risk Assessment

This section presents an updated risk assessment with possible threats, their probability of occurrence during the development of the project and possible actions to mitigate them.

3.1 Not enough resources on selected FPGA

Probability: High
Impact: Medium-Low
Initial Mitigation Strategy: On a later phase of the development, there is a high probability that the FPGA resources are not enough to accommodate the required functionality. In most cases this problem has to do with the available logical cells and not the available IO pins. In this case, most of the FPGA manufacturers provide models with the same pinout but with more logical cells, in terms of an increased price. Incorporating an FPGA with the same pinout but more logical cells requires only a few software modifications.
Updated Mitigation Strategy (PDR): The selected FPGA line (ZYNQ-7020) as of Preliminary Design, offers enough resources to accommodate all requirements set for the product. A preliminary design, integrating the peripherals that will be used and various DSP operations (filtering, resampling, FFT) resulted to a resource utilization below 50% as Figure 3.1 shows. The final bitstream may greatly vary, but this is a good indication about the capabilities of the FPGA. In addition, some of the less time-critical operations can be offloaded by the on-chip ARM processors.

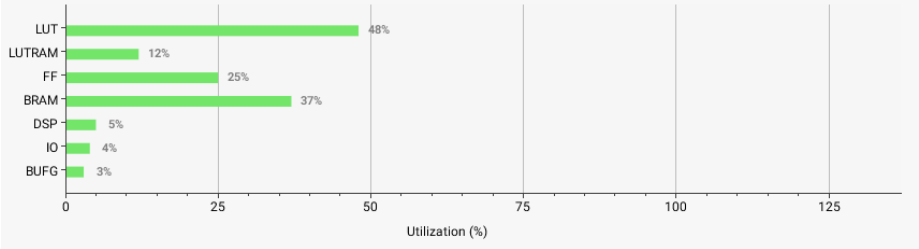

Figure 3.1: ZYNQ-7020 resource utilization Vivado report

3.2 MCU mis-behavior due to EMI

Probability: Medium
Impact: Medium
Initial Mitigation Strategy: Due to the small factor and high transmit power, there is a possibility of the MCU to malfunction due to excess EMI. This can be observed especially in the breadboard models during development. Proper simulations, ground plane planning and shielding should be able to deal with this problem.
Updated Mitigation Strategy (PDR): Initial placement of components as of Preliminary Design is taking this risk into account. More simulations are needed towards the Critical Design milestone.

3.3 RF components matching

Probability: High
Impact: High
Initial Mitigation Strategy: Network impedance matching is one of the most common problem in RF design and can severely affect the performance of both the reception and the transmission. The small form factor of the proposed COMMS subsystem is also expected to negatively contribute to the matching problem. To mitigate this problem, most of the RF components required will be selected to be already matched in the target 50Ω impedance. This will eliminate ambiguities in the matching network and simplify the overall PCB design.
Updated Mitigation Strategy (PDR): Careful design and selection of components for the RF networks has been employed as evident in the Preliminary Design. More simulations are needed towards the Critical Design milestone.

3.4 RF emissions fail to meet the regulatory requirements

Probability: Medium
Impact: High
Initial Mitigation Strategy: At the final stages of the PCB development and during the testing phase, there is a chance that the emissions of the transmitter may not meet the regulatory requirements, causing interference to adjacent channels etc. This normally occurs after the signal amplification. To mitigate this risk, excessive simulations will be performed during the development phase and testing at each iteration to ensure compliance. In addition, hardware integrated components will be preferred, over custom solutions due to their predictable and documented performance characteristics.
Updated Mitigation Strategy (PDR): Careful design and selection of components for the RF networks has been employed as evident in the Preliminary Design. More simulations are needed towards the Critical Design milestone.

3.5 Software integration issues

Probability: High
Impact: High
Initial Mitigation Strategy: A major problem during software development of new systems, is the final integration into a single entity. Due to the size and the complexity of the proposed COMMS subsystem, final software integration may reveal software bugs. To avoid them quality assurance and coverage tests will be employed in every software component, throughout the entire software development process.
Updated Mitigation Strategy (PDR): No updates for the Preliminary Design milestone.

3.6 Doppler offset exceeds channel capabilities of the RF IC

Probability: High
Impact: Low
Initial Mitigation Strategy: Frequency drift due to the doppler effect, especially in LEO channels, varies from few kHz up to 60 kHz in case of the S-band. This can be an issue for RF ICs and the overall receiver design. A possible solution could be to increase the filter bandwidth of the receiver, but this of course would have a negative impact to the performance and sensitivity. We are planning to mitigate this issue with the help of the ground segment. The ground station prior the transmission will calculate the relative velocity delta, and alter the transmission frequency properly, so the observed frequency at the COMMS receiver after the doppler shift, to lie inside the passband of the filter bandwidth.
Updated Mitigation Strategy (PDR): No updates for the Preliminary Design milestone.

3.7 Network latency issues in handover proxy mode

Probability: Medium
Impact: Low
Initial Mitigation Strategy: During C&C, network latency can become an issue. This situation would be more intense on handover proxy mode via SatNOGS Network in which data are relayed between stations. Latency manifests itself as slow response on commands while in extreme situations it can even render the whole C&C session useless. The mitigation action for this issue is to forbid handover sessions in proxy mode for high data rate communications and bands like the S-Band. Low data rate UHF communication can still utilize the proxy mode and benefit on the simpler network connection configuration it requires.
Updated Mitigation Strategy (PDR): No updates for the Preliminary Design milestone.